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Generation of Hardware Emulation Platform for Multi-FPGA Based NoC



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Background

Multi-FPGA based emulation platform for NoC (Network-on-Chip) gives a solution to the resource limitation of single FPGA based emulation platform. The generic design flow is needed to generate the emulation architecture for multi-FPGA based NoC. **Objective**

We propose a design flow that generates multi-FPGA based NoC. With the routing IP library for multi-FPGA based 3D NoC, the platform specification, the data transfer specification and emulation blocks, the generation tools can automatically generates a hardware emulation platform for multi-FPGA based NoC.

Architecture of the multi-FPGA based

S: Source Node D: Destination Node C: Current Node

GUI of the generation tools

(developed with python)

NoCgen: the NoC Generation Tool		
		Help
About NoCgen	NoC Generation tool	Hermes files directory Hermes NoC library directory NoC_LIB Destination NoC directory
ype of NoC		
3D_Asyn 💌 Nu	umber of FPGAs 2 🚊	
Courting Algorithm	~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~	
• XY • WFM • NLM	O NFM O W	FNM C NLNM C NFNM
XY O WFM O NLM mulation environment	O NFM O W	FNM ONLNM ONFNM
● XY ○ WFM	ONFM OW	FNM ONFNM
● XY ● WFM ● NLM mulation environment ■ Emulate ● Automatic load	ONFM OW	FRIM O NILRIM O RENM
● XY ○ WFM	ONFM OW	FNM ONENM
● XY ● WFM ● NLM mulation environment ■ Emulate ● Automatic load	O NFM O W	FRIM O RILRIM O RFRIM
● XY ● WFM ● NLM mulation environment ■ Emulate ● Automatic load ● multi-destination ● One-destination	ONFM OW	FRIM C HILINM C HF/HM
● XY ● WFM ● NLM mulation environment ■ Emulate ● Automatic load ● multi-destination		FRUM O NILBUM O NIFUM
 ♥ Y ♥ WFM ♥ Emulate ○ Automatic load ○ multi-destination ○ One-destination Data transfert scenario □ From NoC library 		
 ● XY ● WFM ● NLM ■ mulation environment ○ Automatic load ○ multi-destination ○ One-destination ■ Data transfert scenario □ From NoC library ○ (元) ○ 編辑 		
 ● XY ● WFM ● NLM ■ mulation environment ✓ Emulate ○ Automatic load ○ multi-destination ○ One-destination ■ Data transfert scenario □ From NoC library ④ (元) ④ 編辑 		

 Z_N : the index of the FPGA that node N belongs to

*N*_{MD}: Multi-dimension Node



Features of multi-FPGA based NoC

Routing algorithm

Support various routing algorithm, such as XYZ,
 NLM_MD, WFM_MD, NFM_MD in multi-dimension
 ➤ Data transfer

Zhiwei Ge: bourse région Rhône Alpes accueil doc 2011 (LaHC-Tianjin) Junayn Tan: bourse région Rhône Alpes 2007-2011 (TIMA-LaHC) One source, one destination
Multi-source, one destination
One source, multi-destination
Multi-source, multi-destination
GALS (each FPGA has its own frequency)
With the globally asynchronous locally synchronous technique can get the latency info for each clock domain

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