Generation of Hardware Emulation Platform for Multi-FPGA Based NoC

Zhiwei GE[1], *Junyan TAN*[2], *Virginie FRESSE*[2], *Frédéric ROUSSEAU*[3], *Suying YAO*[1]
[1]ASIC Design Center, Tianjin Unversity, [2]Laboratoire Hubert Curien, Université Jean Monnet,
[3]TIMA Laboratory

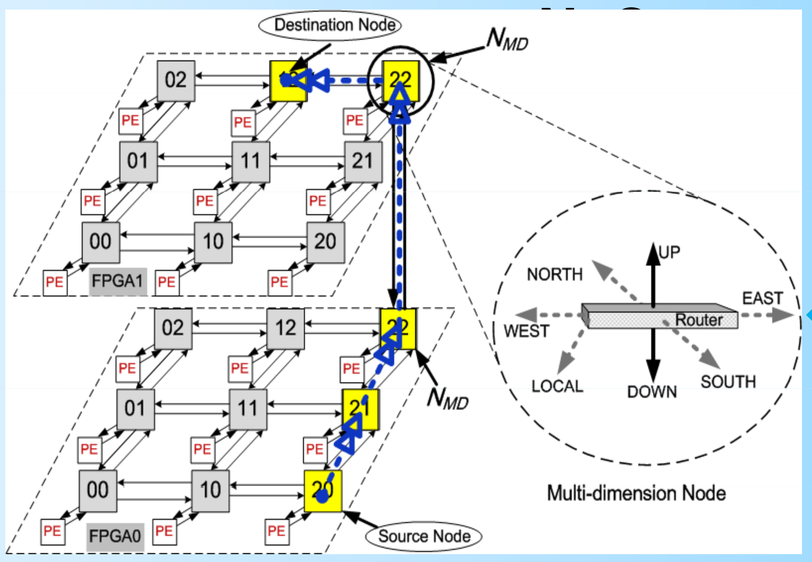
Background

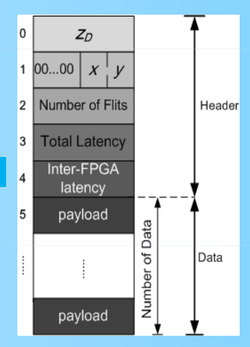
Multi-FPGA based emulation platform for NoC (Network-on-Chip) gives a solution to the resource limitation of single FPGA based emulation platform. The generic design flow is needed to generate the emulation architecture for multi-FPGA based NoC.

Objective

We propose a design flow that generates multi-FPGA based NoC. With the routing IP library for multi-FPGA based 3D NoC, the platform specification, the data transfer specification and emulation blocks, the generation tools can automatically generates a hardware emulation platform for multi-FPGA based NoC.

Architecture of the multi-FPGA based





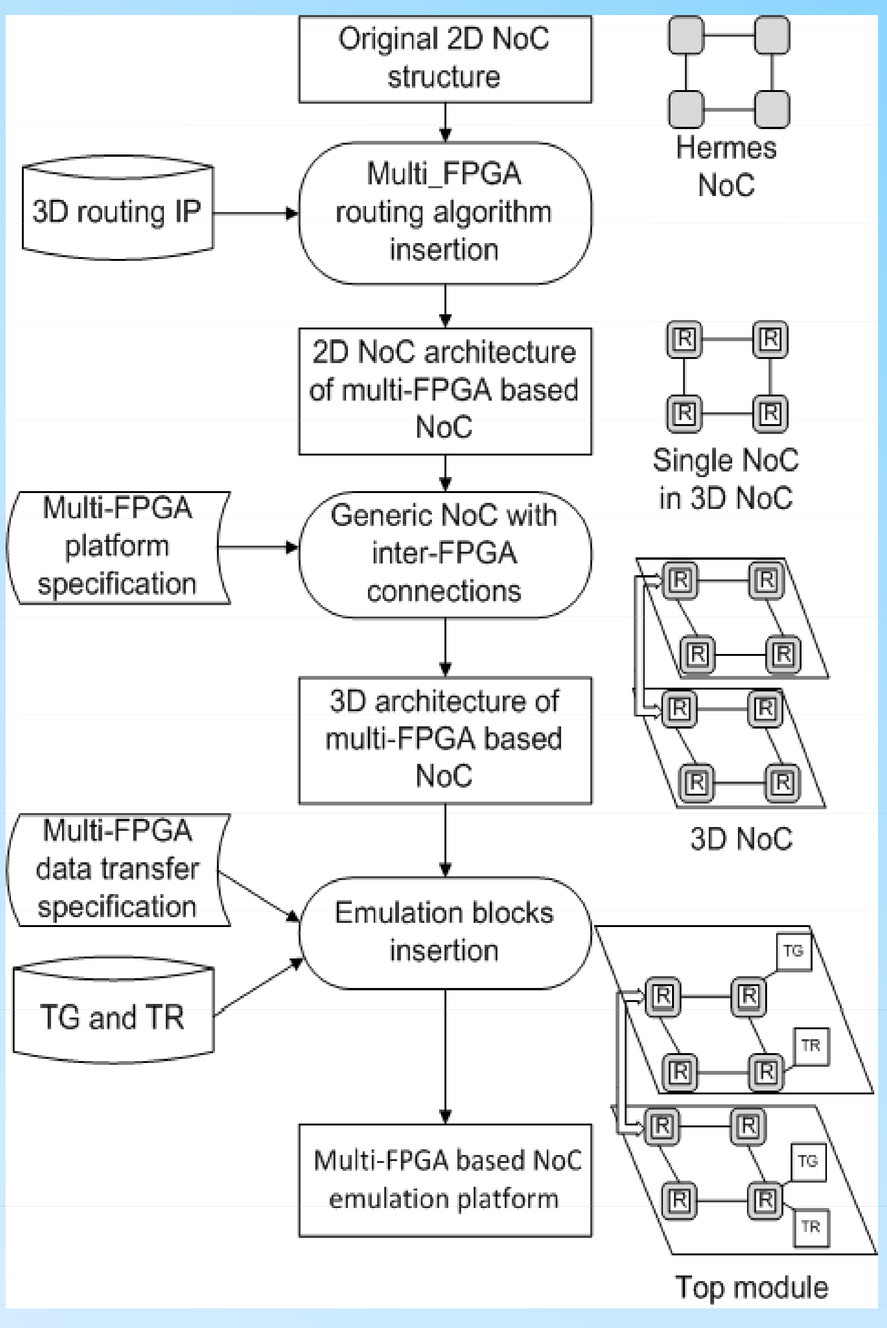
Packet

S: Source Node *D*: Destination Node *C*: Current Node

z_N: the index of the FPGA that node *N* belongs to

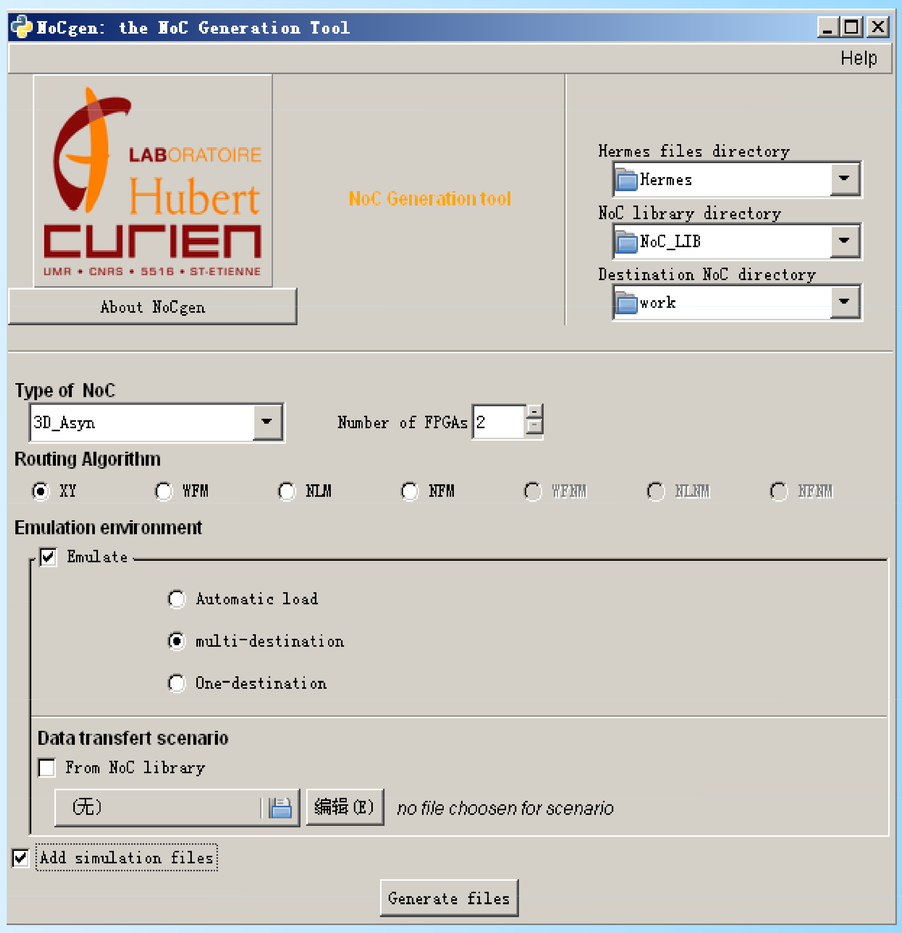
N_{MD}: Multi-dimension Node

Design flow



GUI of the generation tools

(developed with python)



http://tima-sls.imag.fr/www/research/nocgen

Features of multi-FPGA based NoC

- Routing algorithm
  - Support various routing algorithm, such as XYZ, NLM_MD, WFM_MD, NFM_MD in multi-dimension
- Data transfer
  - One source, one destination
  - Multi-source, one destination
  - One source, multi-destination
  - Multi-source, multi-destination
- GALS (each FPGA has its own frequency)
  - With the globally asynchronous locally synchronous technique can get the latency info for each clock domain

Zhiwei Ge: bourse région Rhône Alpes accueil doc 2011 (LaHC-Tianjin)
Junayn Tan: bourse région Rhône Alpes 2007-2011 (TIMA-LaHC)