3D Network on Chip on 3D Chip

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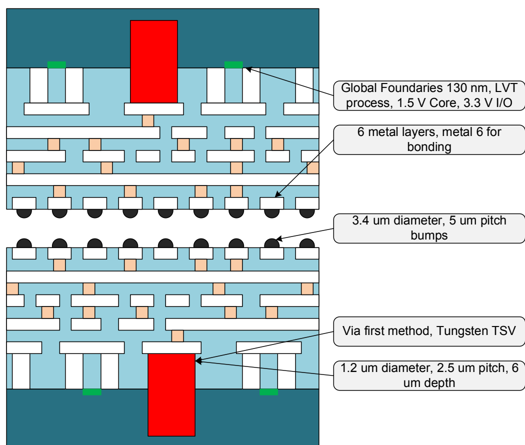
Motivations

- state of the art of 3D implementation [2] [3] [4] [5] [6] does not consider complete multiprocessor with NoC architecture
- how much performance improvement (speedup, execution cycles) of parallel application in 3D architecture

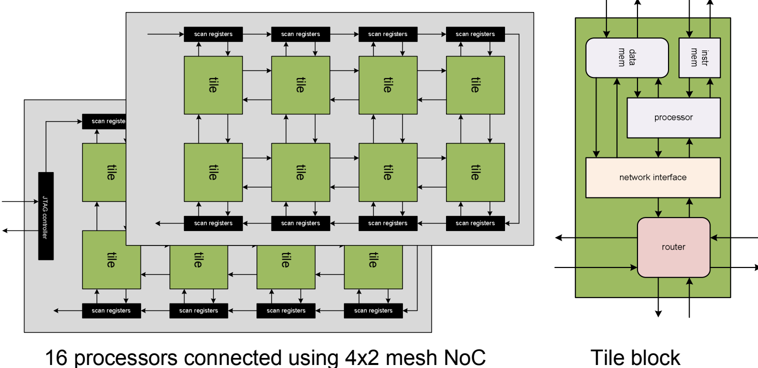
Objectives

- to demonstrate complete multiprocessor with 3D NoC architecture
- to propose a design methodology for exploring multiprocessor design in 3D
- to evaluate performance improvement of parallel applications in 3D NoC architecture

3D Technology



Two tier 3D stacking

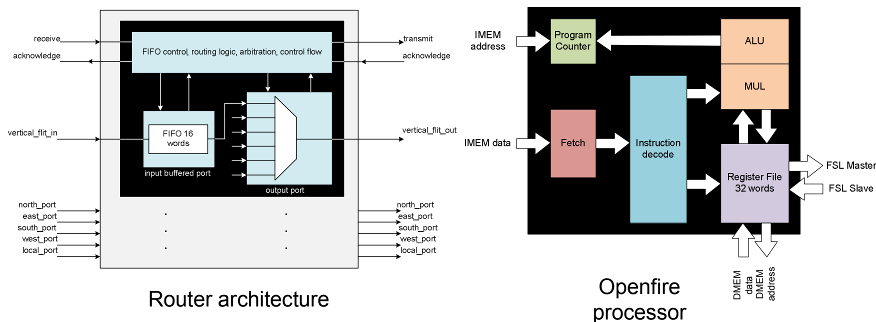


16 processors connected using 4x2 mesh NoC

Tile block

3D Architecture

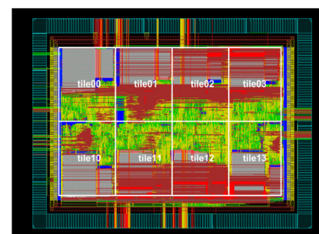
- Target operational frequency = 147 MHz (7 ns clock), target test frequency = 10 mHz
- Fully synchronous, off-chip interface using JTAG IEEE 1149.1
- Die size = 5.0 mm x 3.5 mm



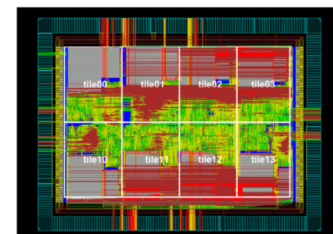
Router architecture

Openfire processor

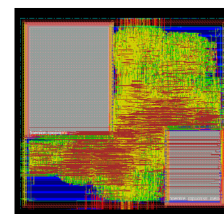
Physical Implementation



Top tier



Bottom tier



Tile layout

References

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[4] Van der Plas et al, "**Design issues and considerations for low-cost 3D TSV IC technology**," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, pp.148-149, 7-11 Feb. 2010

[5] Loi, I. et al, "**3D NoCs — Unifying inter & intra chip communication**," *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*, pp.3337-3340, May 30 2010-June 2 2010

[6] Mineo, C., "**Inter-die signaling in three dimensional integrated circuits**," *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, pp.655-658, 21-24 Sept. 2008