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Design for low cost test of RF circuits and systems

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Outline

- Introduction
  - Challenges in RF test
  - Alternatives to specification-based test
- Built-in test combined with alternate test
- Case study: 2.4 GHz CMOS LNA
- Built-in sensors
  - Dummy structures and PCMs
  - DC probes
  - Envelope Detector
  - Current Sensor
- Alternate test and fault coverage results
- Conclusions and future work

Challenges in RF test

- High cost Automatic Test Equipment (ATE)
- Long test times due to:
  - Large number of RF performances
  - Sequential approach to test each performance (switching between test configurations, application of test stimuli, settling time, pure electrical test time)

- Increasing complexity (SoC, SiP)
- Signal integrity requirements
- Calibration and de-embedding

Alternatives to Specification-Based Test

- **Structural test** [E. Acar et al., *IEEE Trans. Compu.–Aided Des. Integr. Circuits Syst. 2008*]
  - Definition of electrical faults using IFA
  - Select test vectors to detect the presumed faults
  - Lack of a widely acceptable analog fault model

- **Built-off test**
  - Migrate some of the complex functions of the tester onto the test board (i.e. test stimulus generators, modulator, demodulator etc.) [S. S. Akbay et al., *IEEE Trans. on adv. Packaging 2004*]
  - In-house test board development is challenging

Alternatives to Specification-Based Test (cont'd)

- **Built-in test**
  - **Miniature tester on-chip** [M. G. Mendez-Rivera et al., *J. Electron. Test 2005*]
  - **Reconfigure the device under test into a more testable form** [G. Huertas et al., *IEEE Des. Test Comput. 2002*]
  - **Add on-chip sensors** [S.S Akbay et al., *IEEE VLSI Test Symp. 2005*] [M.Cimino et al., *IEEE J. of Solid State Cir. 2008*]

- **Alternate/Machine-Learning-Based Test**
  - **Finds the mapping between low-cost measurements and performances**
  - **Performance prediction** [P.N. Variyam et al., *IEEE Trans. Compu.–Aided Des. Integr. Circuits Syst. 2002*]
  - **Go/No-Go test** [H. Stratigopoulos et al., *IEEE Trans. Compu.–Aided Des. Integr. Circuits Syst. 2008*]

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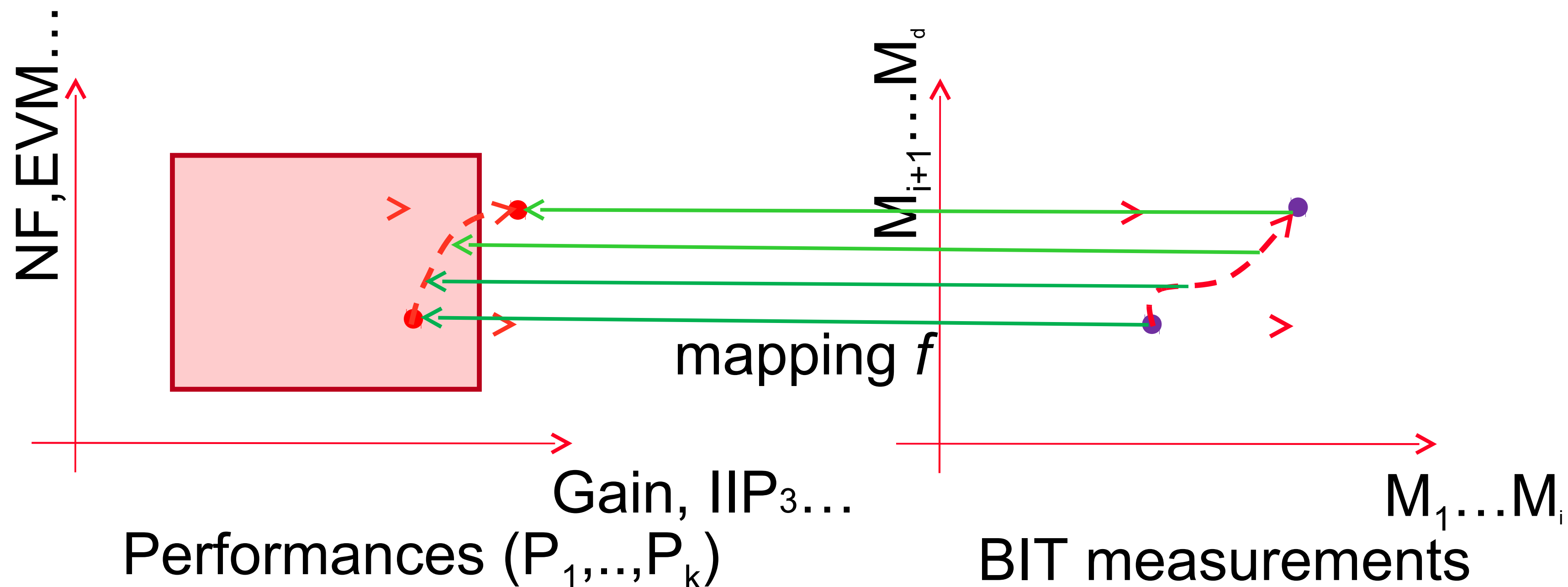
Why Built-in Test (BIT)?

- **Increases the observability of embedded blocks**
- **Offers on-chip low-frequency or DC test signatures**
  - **Clean signal path, good isolation, noise immunity**
  - **DUT connection to inexpensive tester**
- **Performances are tested in parallel (fewer test configurations and test stimuli)**

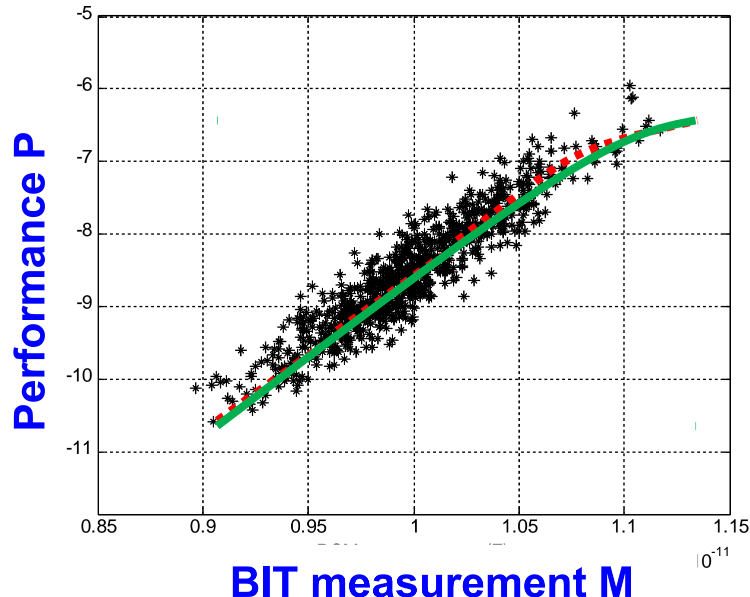
BIT with Alternate Test



- **DUT performances = *f*(BIT measurements)**
- **The analytical expression of *f* is unknown**
- **The BIT measurements are related to the DUT performances in a complex way**

BIT with Alternate Test (cont’d)

- The mapping *f* is modeled using regression functions (alternate test)
- The regression functions are learned based on a representative population of devices with process variations



BIT measurement “tracks” the changes of performance P

Regression function used to predict performance P

Challenges

- BIT measurements should “track” the DUT behaviour
- Built-in sensors should:
  - Incur low area overhead (also minimizes the probability of fault occurrence within the sensor)
  - Be transparent to the DUT
  - Not increase prohibitively the pin count
  - Detect the presence of defects in the DUT

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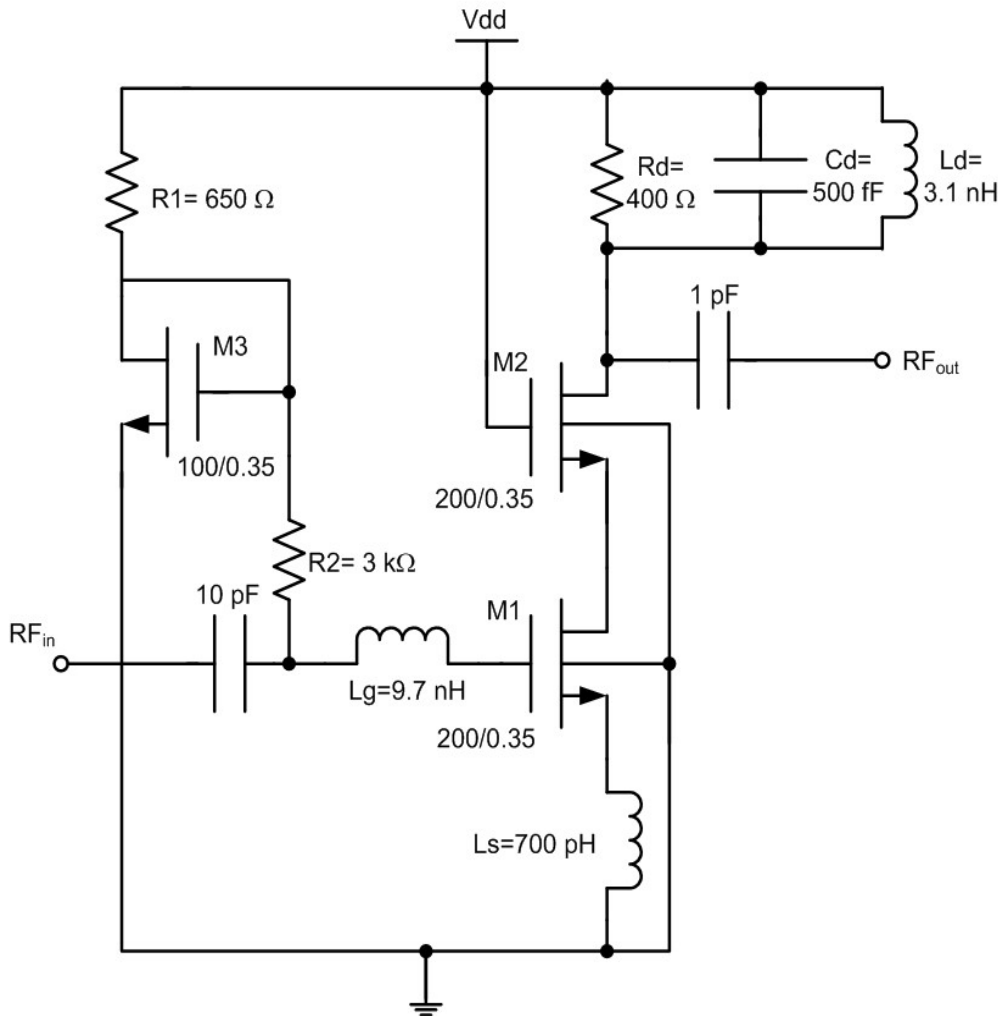
Case Study: 2.4GHz CMOS LNA



Performances	Values
S11 (dB)	-13.51
S12 (dB)	-42.4
S21 (dB)	11.88
S22 (dB)	-8.9
NF (dB)	1.513
IIP1 (dBm)	-11.04
IIP3 (dBm)	5.92

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Built-in Sensors Studied in this Work

Non-connected Sensors

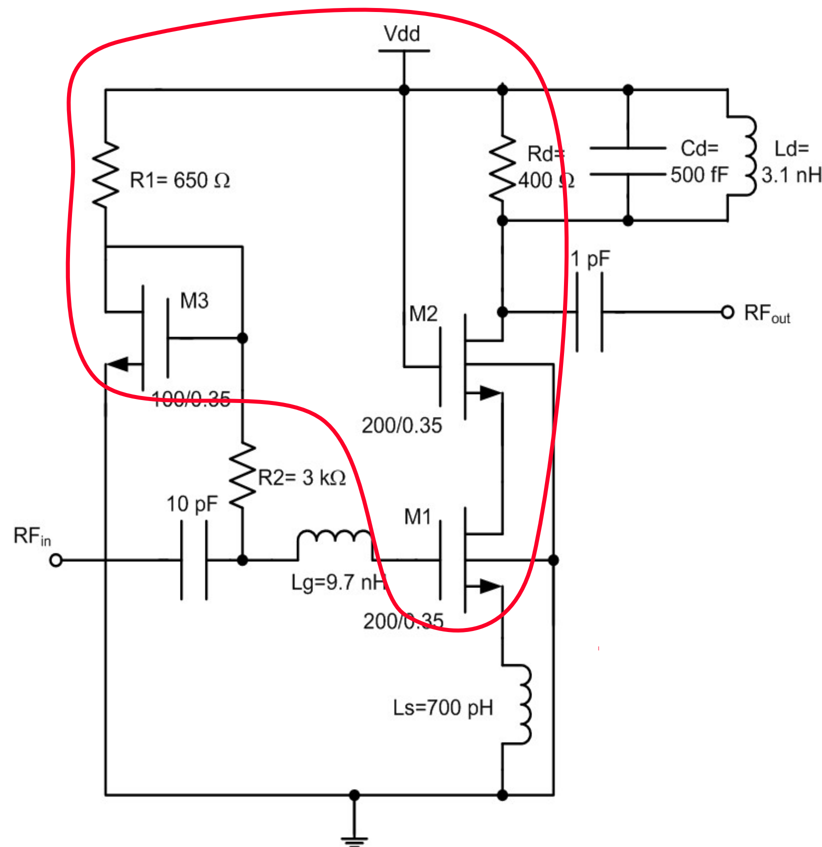
- Dummy Structures & Process Control Monitors (PCM)
  - Non-intrusive
  - They are located in close proximity to the DUT, they "sense" the same process variations with the DUT, thus they track its performances

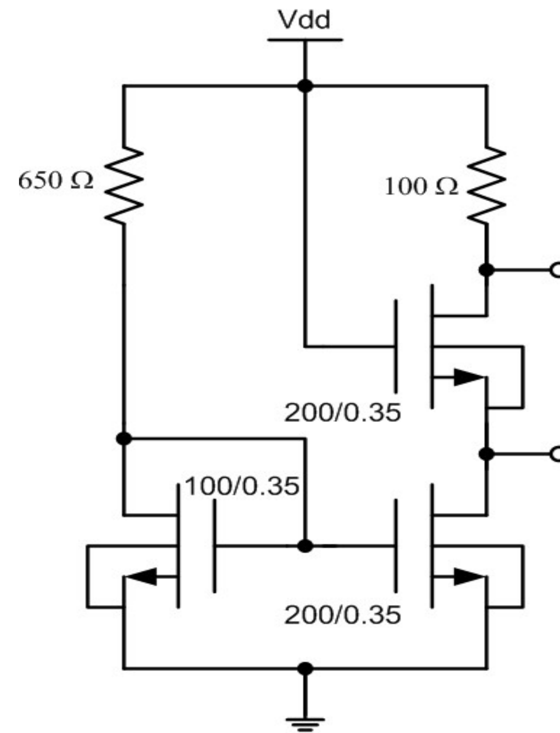
Connected sensors

- DC probes
- Envelope detector
- Current sensor

Dummy Structures

- **Dummy structures are simple BIT circuits which mimic common structures already present in the DUT**

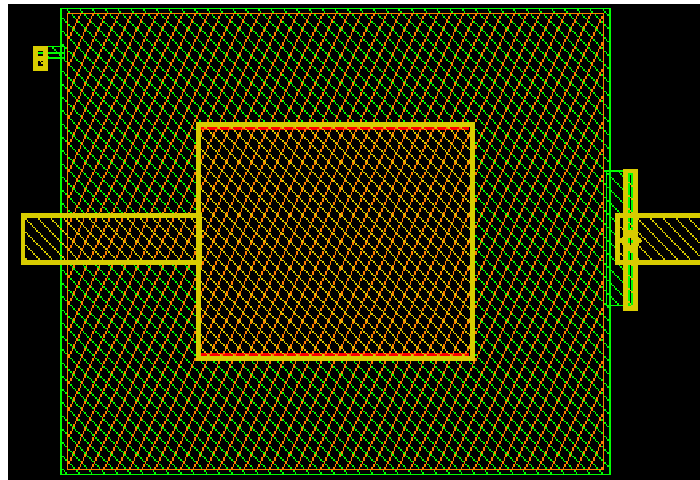




Bias circuit with current mirror

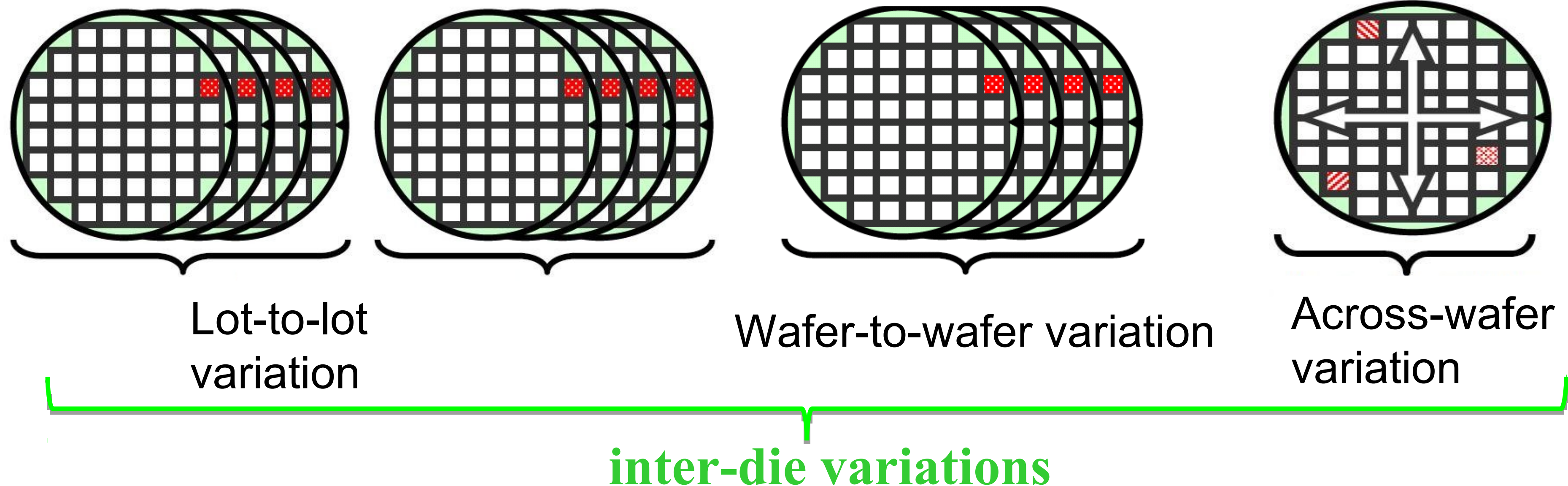
Process Control Monitors (PCMs)

- A PCM is a basic layout component (i.e. capacitor, transistor, etc.)
- We use it to monitor a low-level process parameter (i.e. capacitance per unit area, reverse saturation current for BJTs, etc.)
- In our work, we have used a metal-insulator-metal (MIM) PCM.



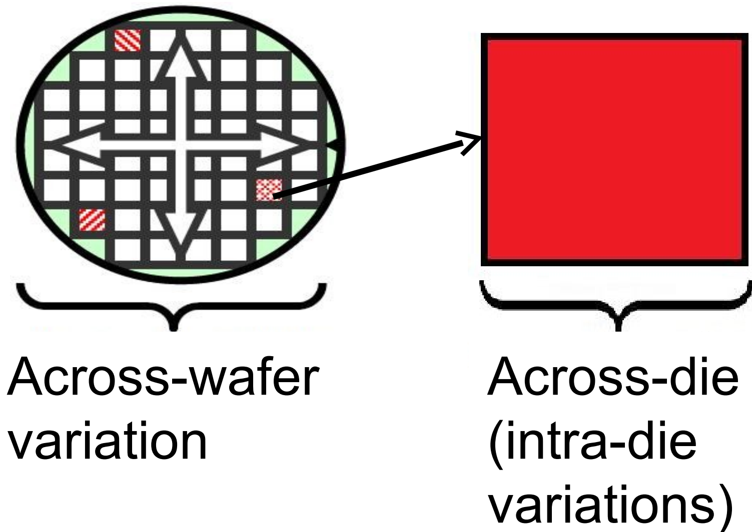
Layout of MIM Capacitor

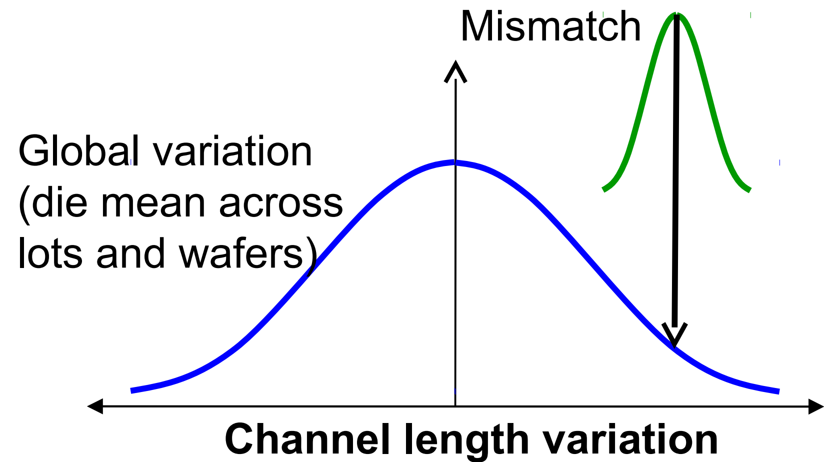
Principle of Operation of Dummy Structures and PCMs



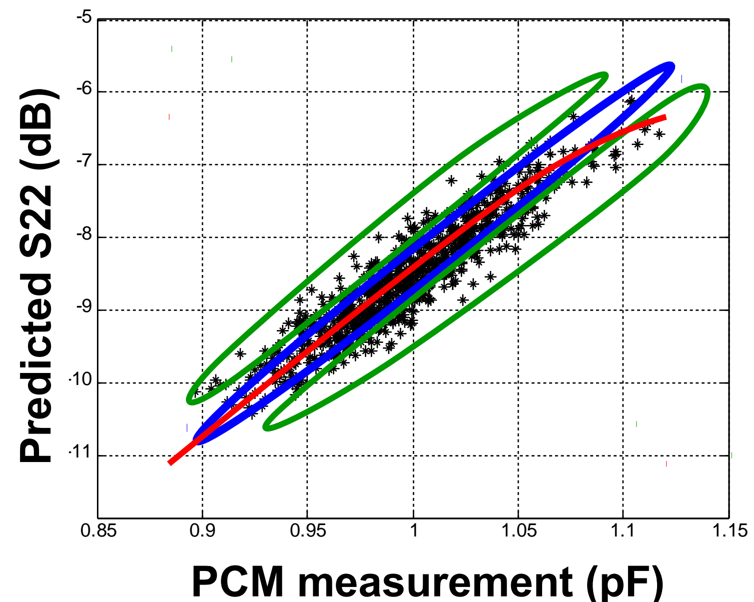
- For a process >100nm, inter-die variations are slow-varying and smooth
- Neighbouring structures within any die are similarly affected
- DUT performances and BIT measurements are correlated

Principle of Operation of Dummy Structures and PCMs (cont'd)



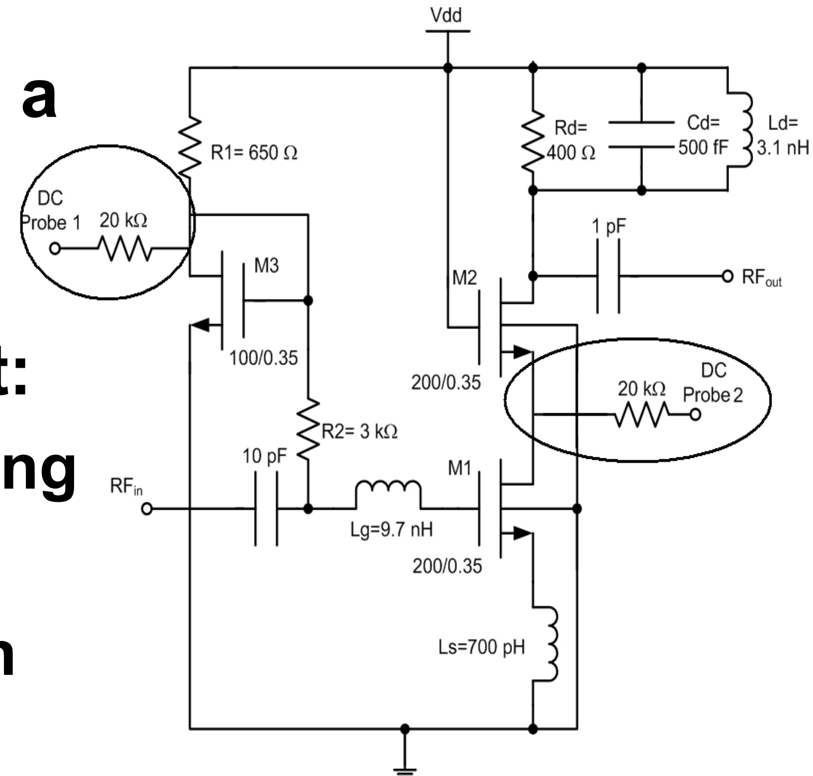


- **Intra-die variations affect the DUT and the BIT structures differently, thus they might corrupt the correlation**
- **Alternate test can moderate this effect**



DC Probes

- A DC probe can be set up by a large resistor
- Two DC probes are placed at:
  - The drain of M3 in the biasing stage
  - The common node between M1&M2
- Drawback: they do not sense degradation in L, C components

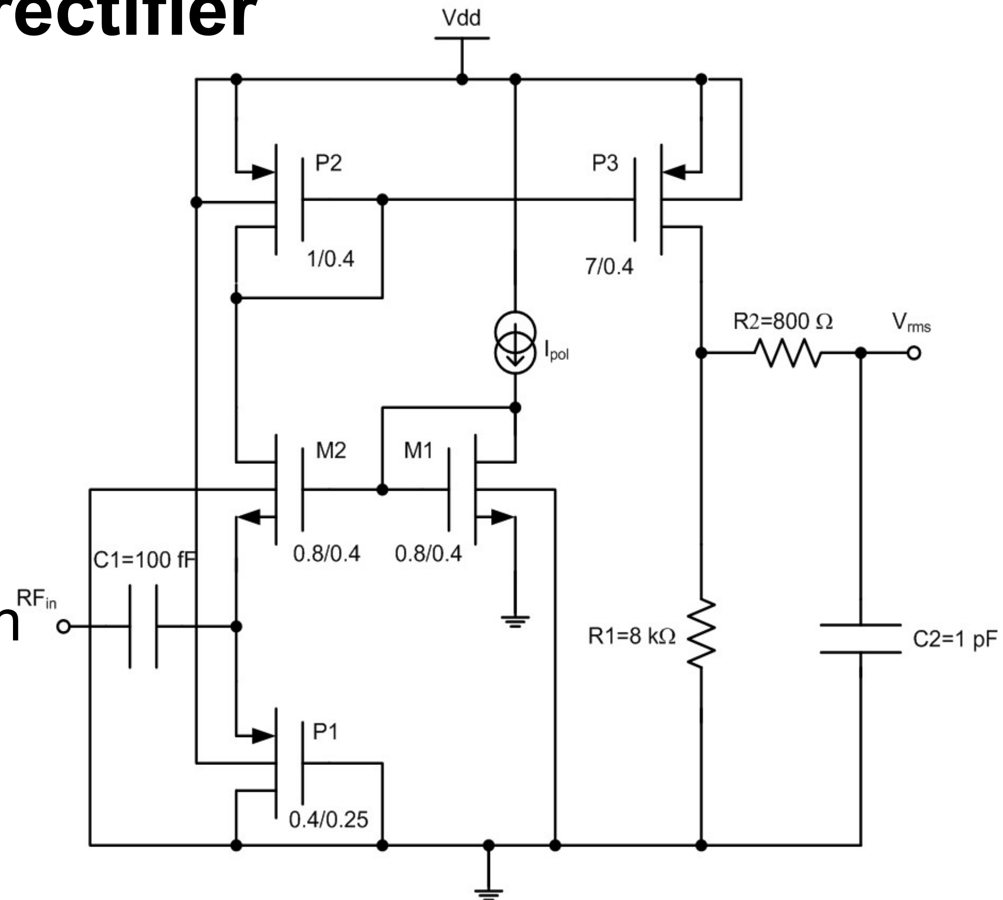


Envelope Detector and Current Sensor

- **Advantages:**
  - Responsive to variations related to L, C, components
  - Low-frequency test signature that carries RF information
- **Challenges/design constraints:**
  - Simple architecture and minimum silicon area overhead
  - High-input impedance (transparent to DUT)
  - High input dynamic range
  - Wide band of operation

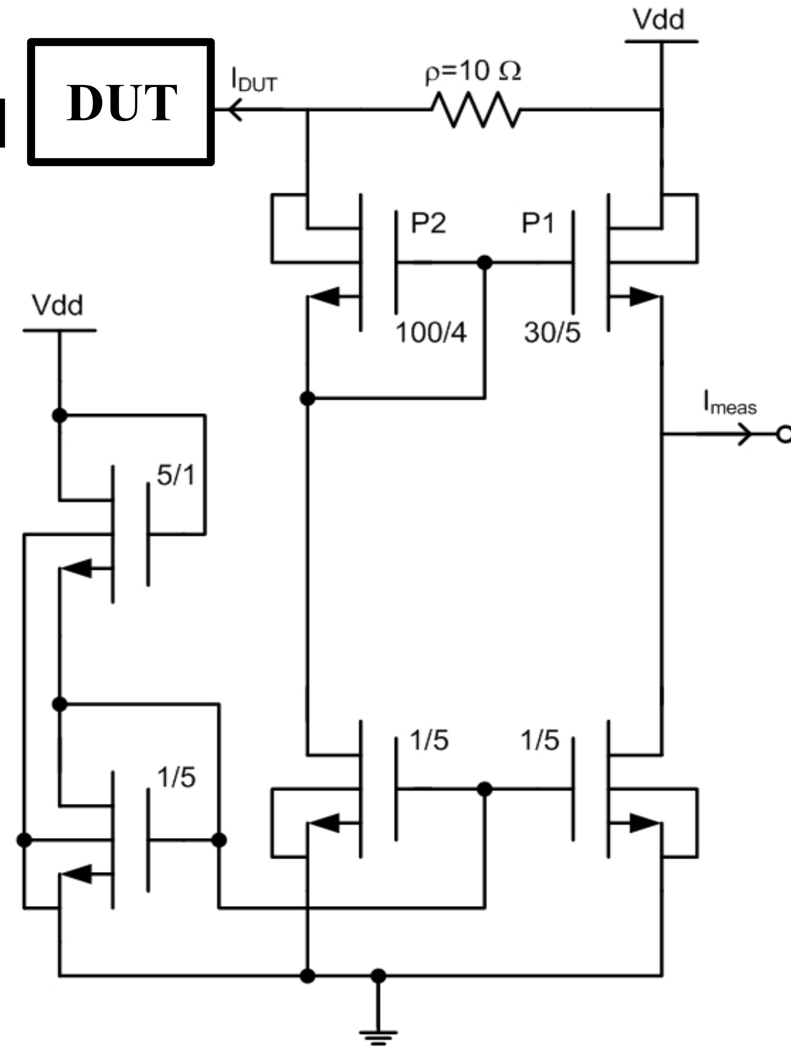
Envelope Detector (ED)

- **1st stage: Half wave rectifier**
  - M2 in weak inversion
  - Bias current I_{pol} follows through M1
  - V_{gs} of M2 close to V_{th}
  - I > 0 : M2 OFF
  - I < 0 : M2 ON
- **2nd stage:** I - V conversion
- **3rd stage:** Low pass filter



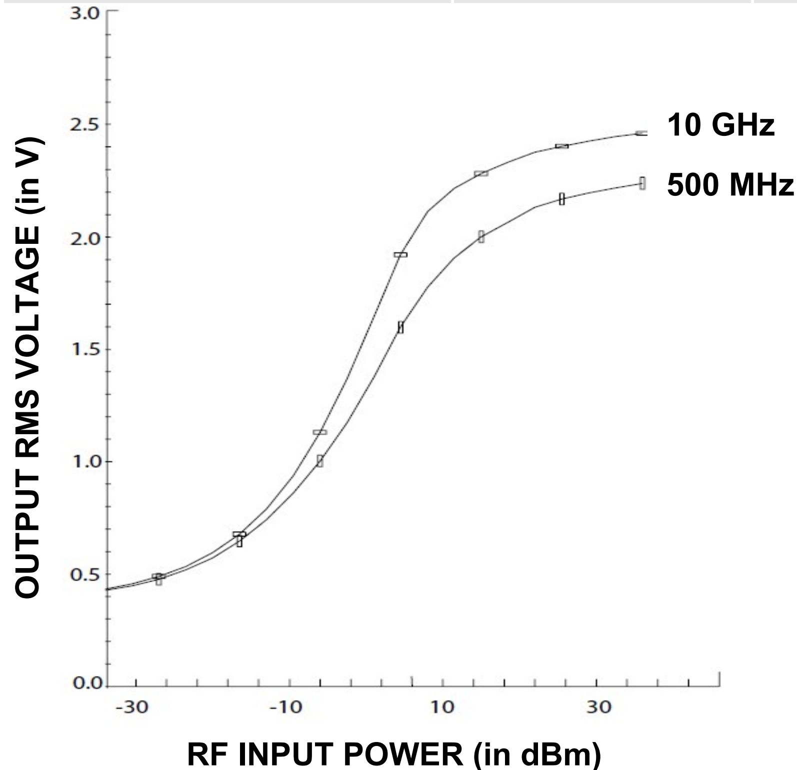
Built-In Current Sensor (BICS)

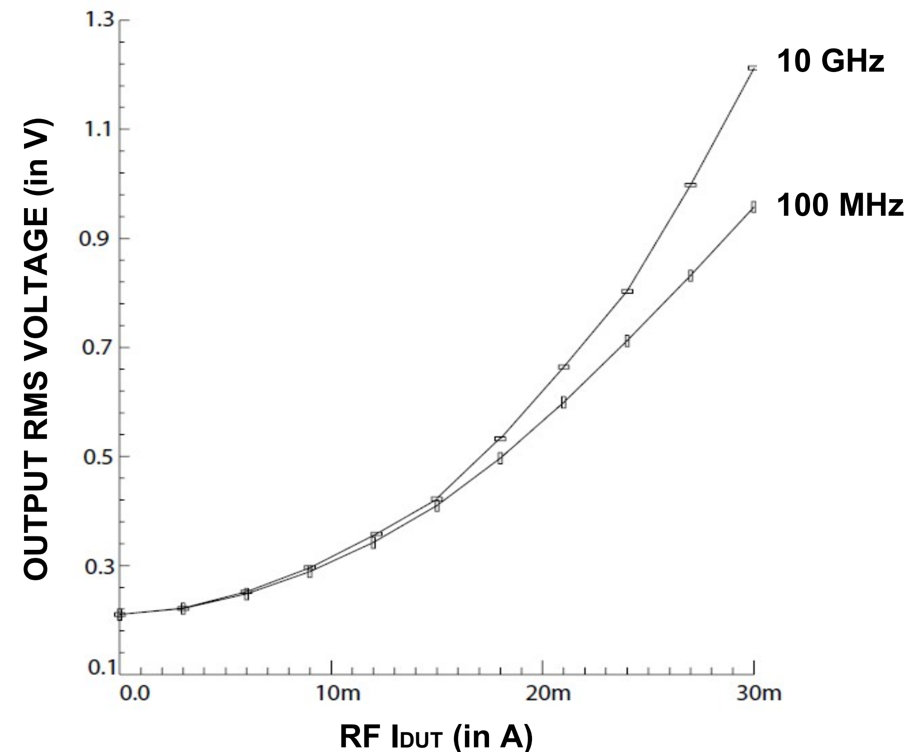
- **Design proposed by**
  [Y. Maidon et al., *Electron. Let. 1997*]
  - Small parasitic resistor ρ provides a voltage drop which unbalances the PMOS current mirror
  - Output current is proportional to the RF power supply current of the DUT
  - Output current is switched to the input of the envelope detector to obtain low-frequency signature



Characterisation of the Envelope Detector and the Current Sensor

	Area (μm^2)	Band of frequency (GHz)	Dynamic range (dB)	Input impedance (kΩ)
Envelope detector	2170 (0.5%)	0.5 – 10	35	1.5 – 11
Current sensor	2190 (0.5%)	0.1 – 10	35.6	----

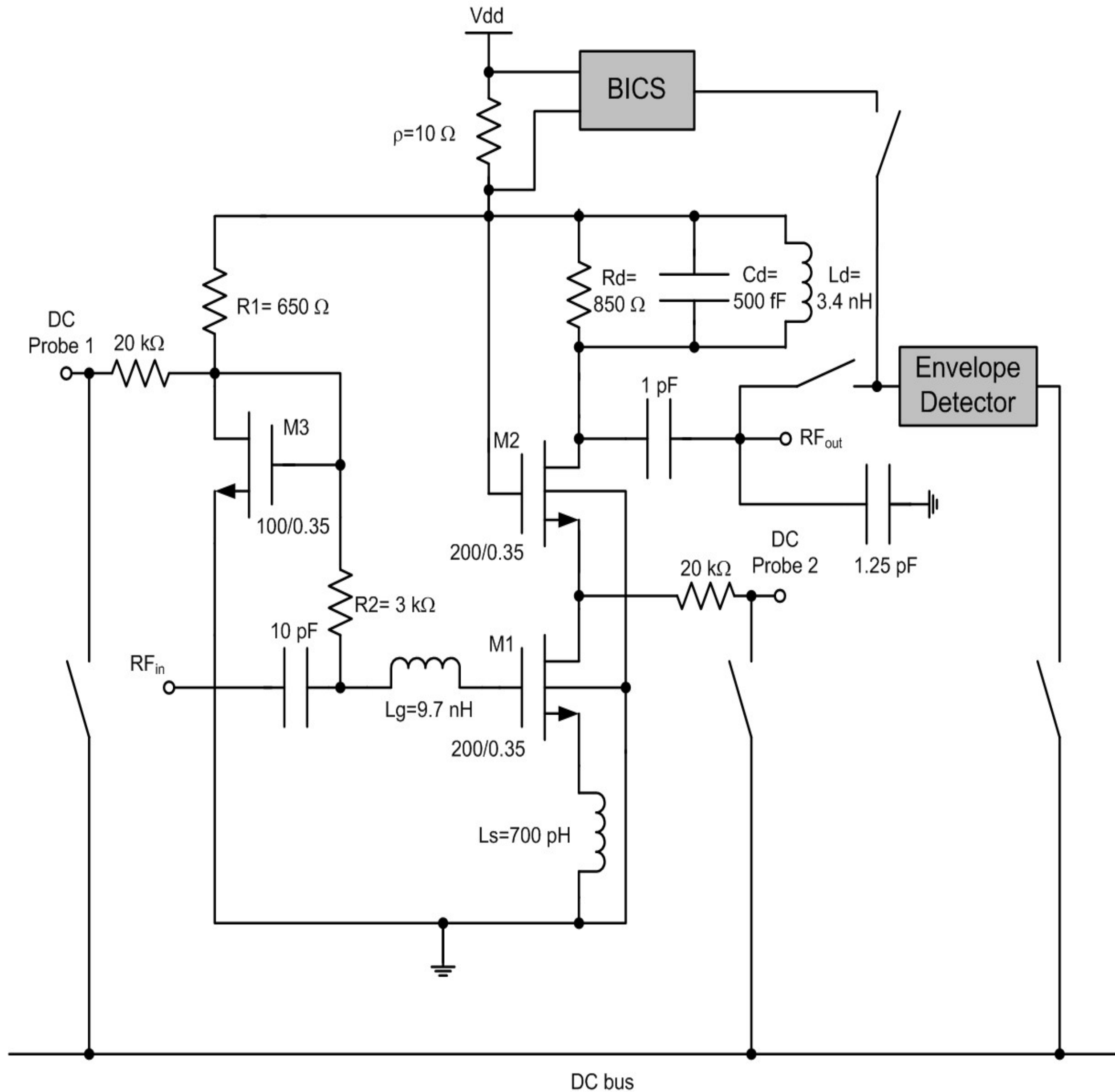




Characterisation of the LNA with BIT Structures

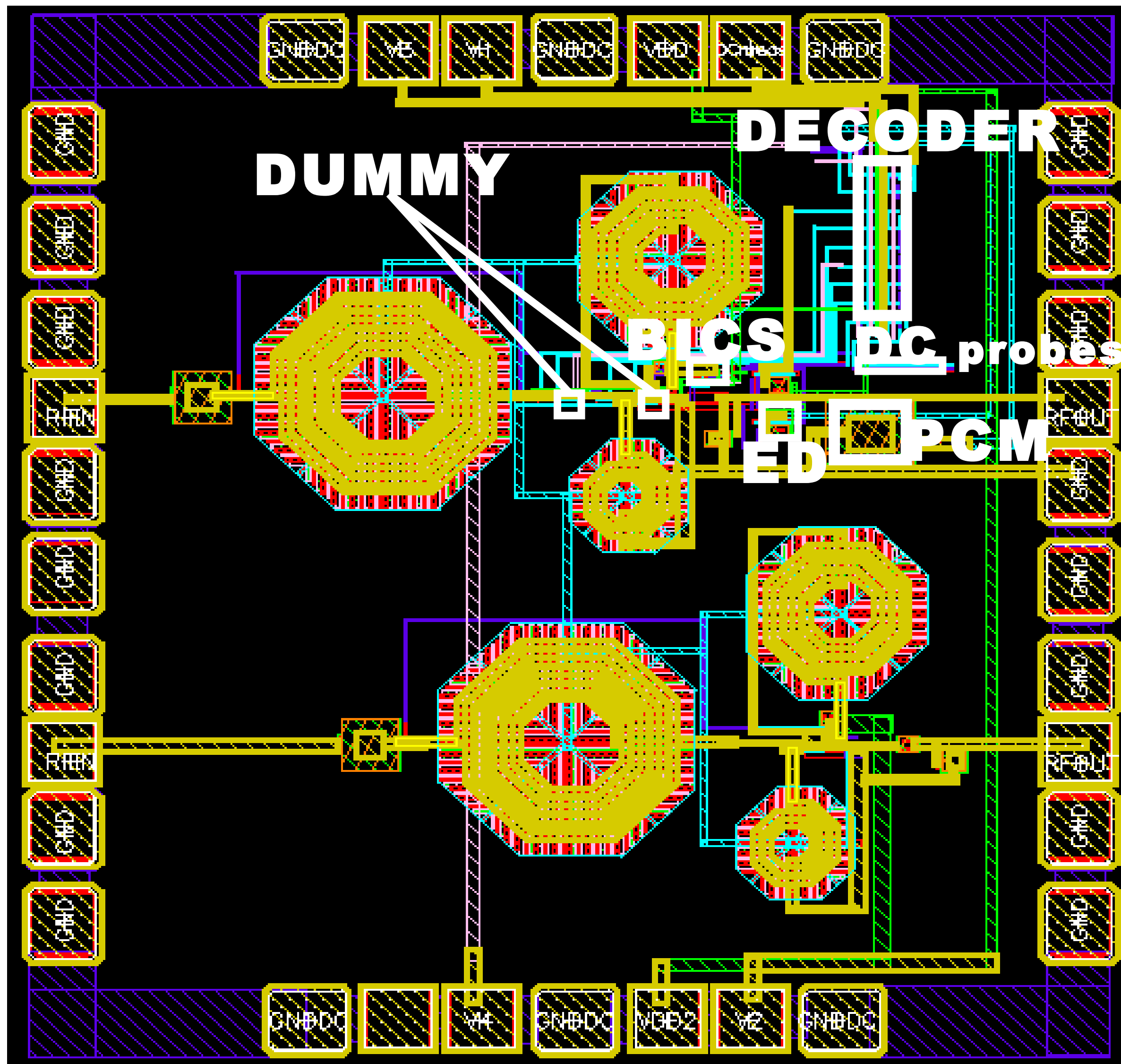
	LNA alone	LNA with ED	LNA with BICS	Co-Design
S11 (dB)	-13.51	+0.01	-0.09	+0.1
S12 (dB)	-42.4	-0.02	+0.7	+0.6
S21 (dB)	11.88	+0.02	-2.18	-0.07
S22 (dB)	-8.9	-0.25	-8.8	-0.4
NF (dB)	1.513	0.01	+0.277	+0.071
IIP1 (dBm)	-11.04	-0.21	-1	+0.013
IIP3 (dBm)	5.92	+0.18	-0.51	-0.14

Co-Design



Layout of the Final Chip

- **Designed with ST Microelectronics 0.25 µm BiCMOS7RF**



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Alternate Test Predictions

- The BIT measurements are mapped to the performances of the LNA using the alternate test paradigm
- Regression functions are trained using 700 post-layout Monte Carlo instances
- The RMS prediction error on an independent validation set (300 Monte Carlo instances) is used to evaluate the alternate test

$$\varepsilon_i = \frac{100}{P_{i,nom}} \sqrt{\frac{\sum_{j=1}^{N} (P_{i,j} - \hat{P}_{i,j})}{N}}$$

	S11	S12	S21	S22	NF	1-dB CP	IIP3
ALL BIT Structures	1.34	0.43	0.70	2.9	1.20	1.4	3.11
Dummy PCM	1.69	0.45	0.93	3.29	1.95	1.78	3.4

RMS prediction errors (in %)

Catastrophic Fault Analysis

- We injected 23 catastrophic faults at the layout level including all possible short- and open-circuits across the components of the LNA
- 17 faults are detected by the two DC probes
- 6 faults are detected by the envelope detector
- Current sensor is unnecessary for this particular model of catastrophic fault

	S11	S12	S21	S22	NF	1-dB CP	IIP3
Dummy PCM DC probes ED	1.41	0.44	0.83	3.1	1.70	1.57	3.23

RMS prediction errors (in %)

Conclusions

- We exploit the existing inter-die variations to predict DUT performances from non-intrusive sensors (dummy structures and process control monitors)
- These sensors "sense" the same variations with the DUT, thus the sensor measurements "track" the DUT performances
- In addition, DC probes, an envelope detector and a current sensor are co-designed with the DUT to detect catastrophic faults injected at the layout level
- The current sensor is unnecessary

Future Work

- **Evaluation of proposed sensors in terms of test escape and yield loss**

  [H. Stratigopoulos et al., IEEE Trans. Compu.–Aided Des. Integr. Circuits Syst. 2009]

- **Expand the library of sensors with emphasis to non-intrusive sensors**

- **Chip fabrication (in the process of transferring the design to a new technology)**

- **Use the same techniques for testing RF systems (receiver, transmitter) in terms of system level specification (BER, EVM)**