Horus: A prototype debug platform for assertion-based design

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TIMA Laboratory

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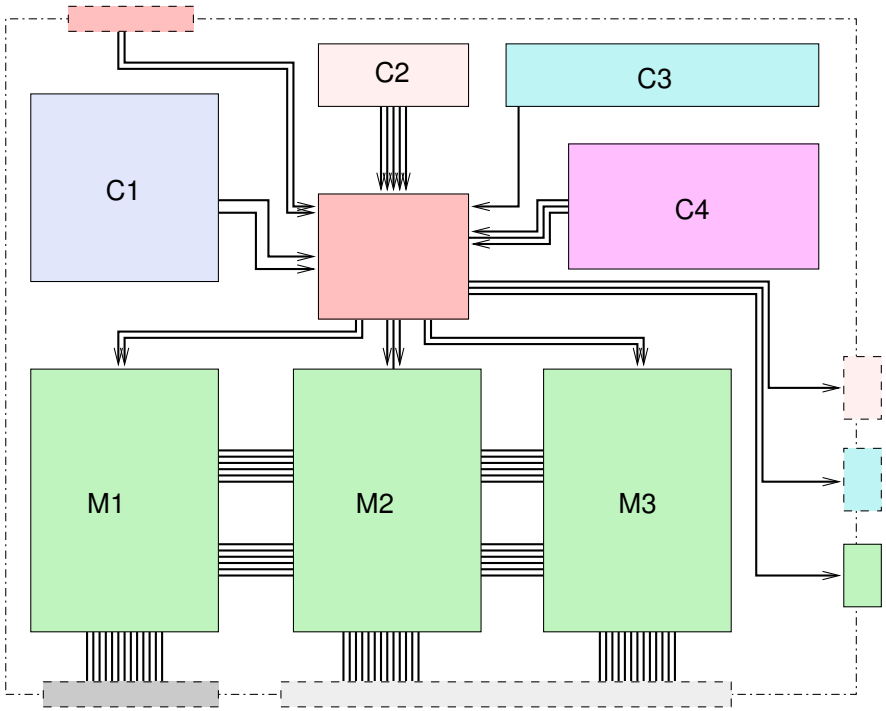
SoC Verification



Assume Guarantee Paradigm

- Properties used to describe
  - environment behavior: assumptions
  - design behavior: assertions

Example

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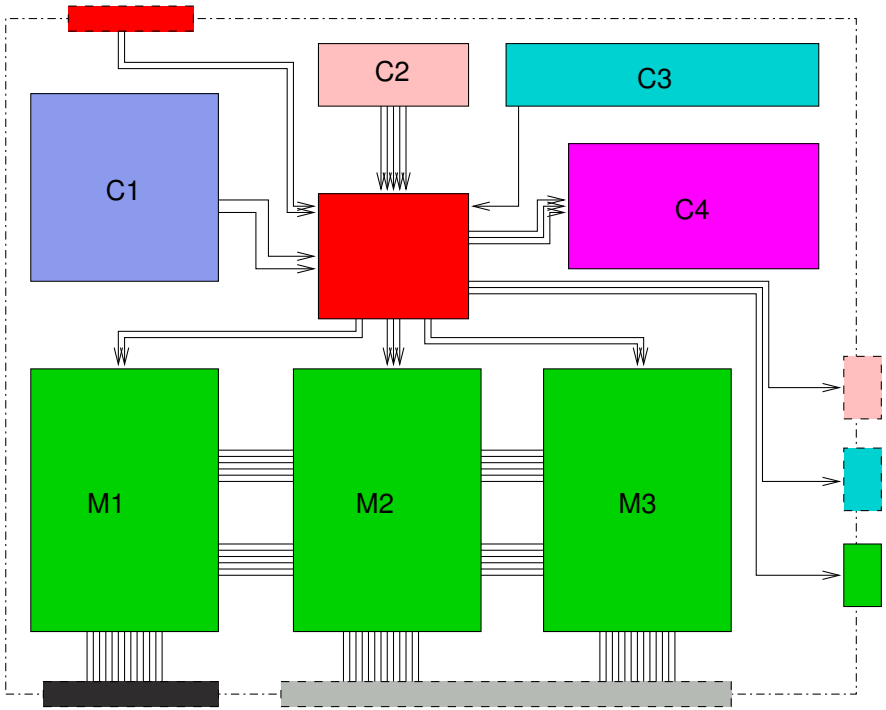
always A ->B before C
```

For on-line testing

Synthesize assumptions and

SoC Verification



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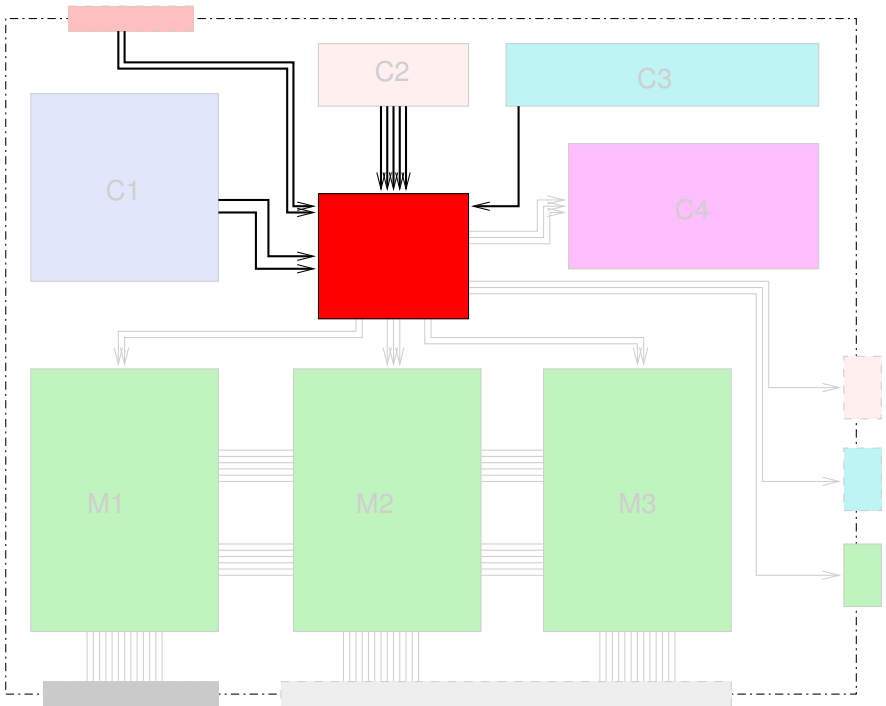

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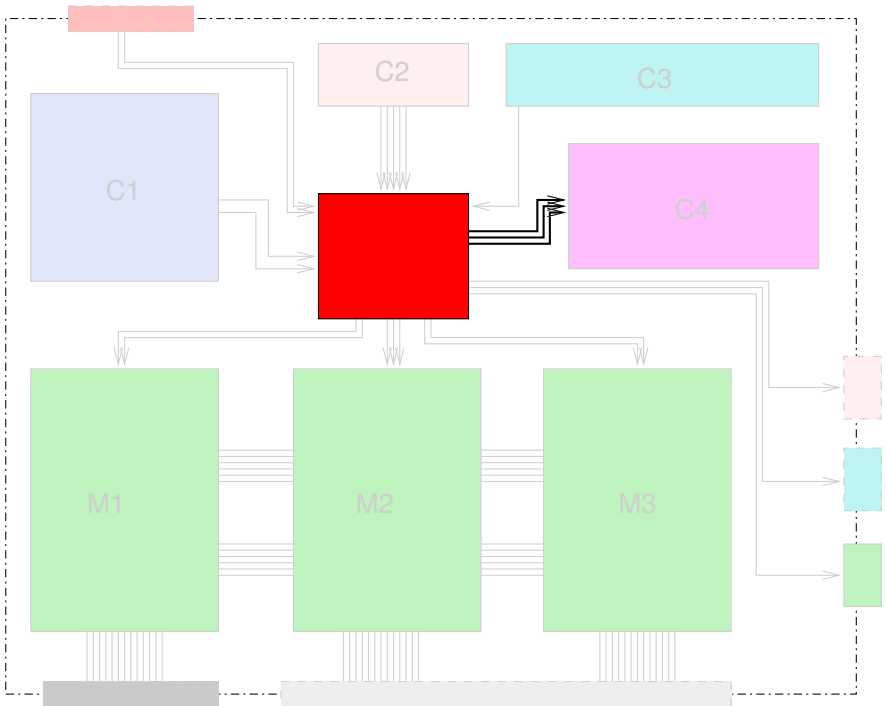

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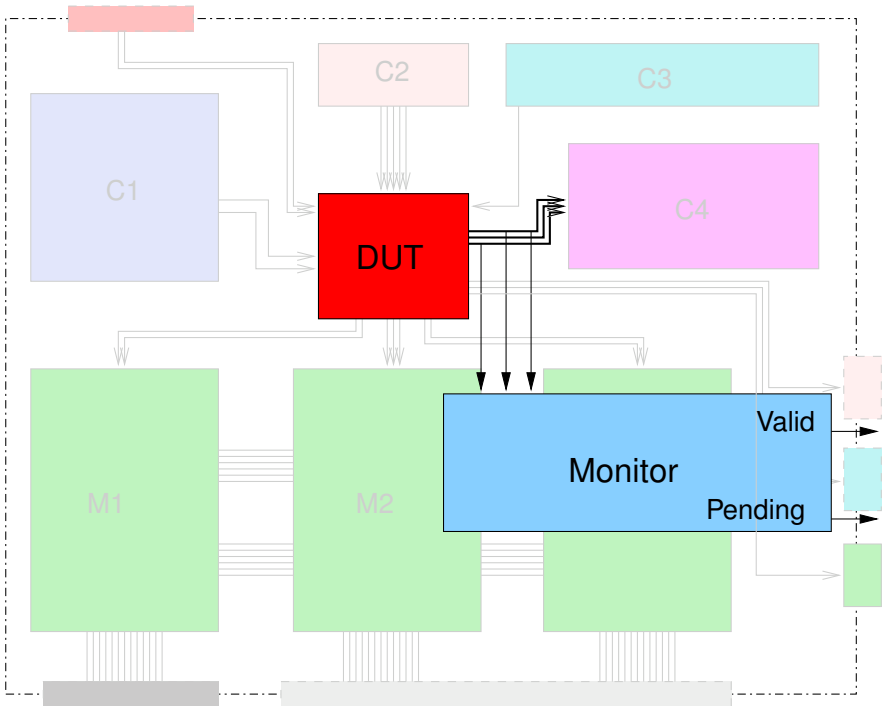

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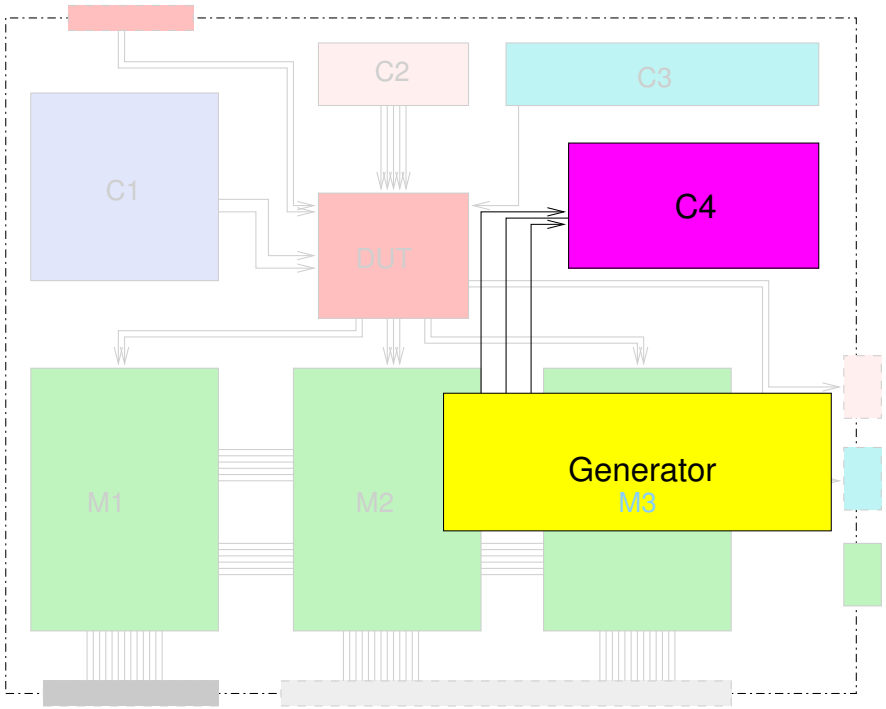

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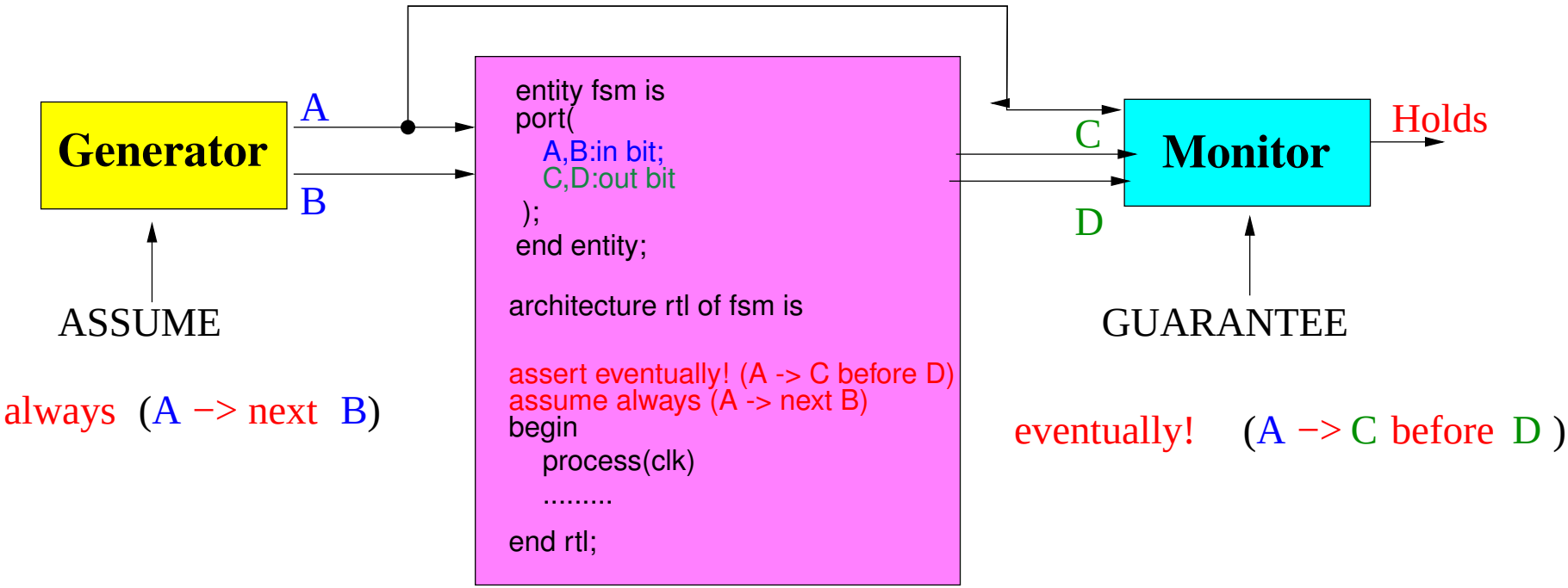
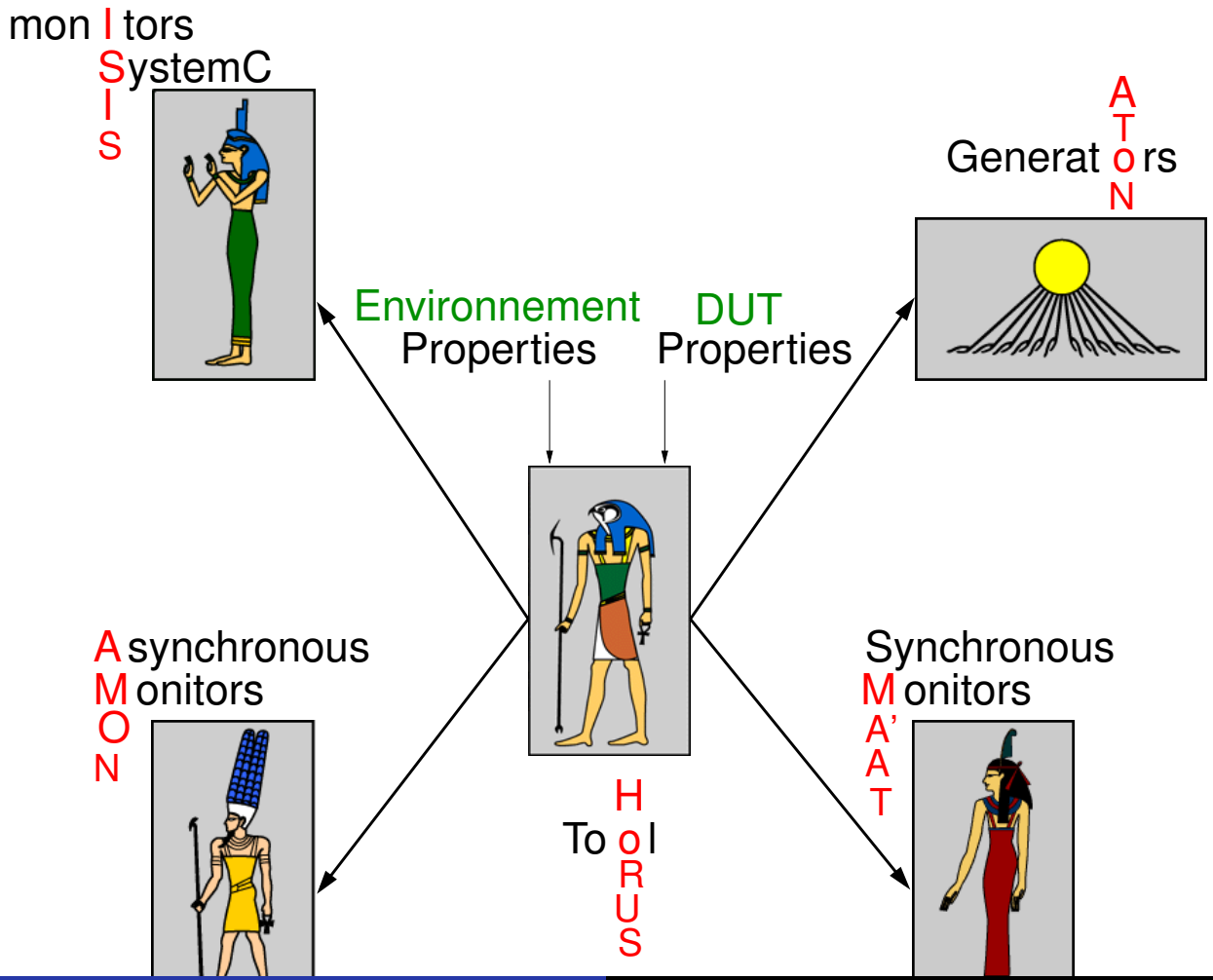
Synthesize assumptions and

Monitors and Generators



Our Global Project



Our Objectives

Monitors or Generators that

- Cover all PSL operator: FL, SERE, boolean layers
- Synthesizable
- Efficient to build: Modular Architecture
- Area Efficient
- Formally proven correct

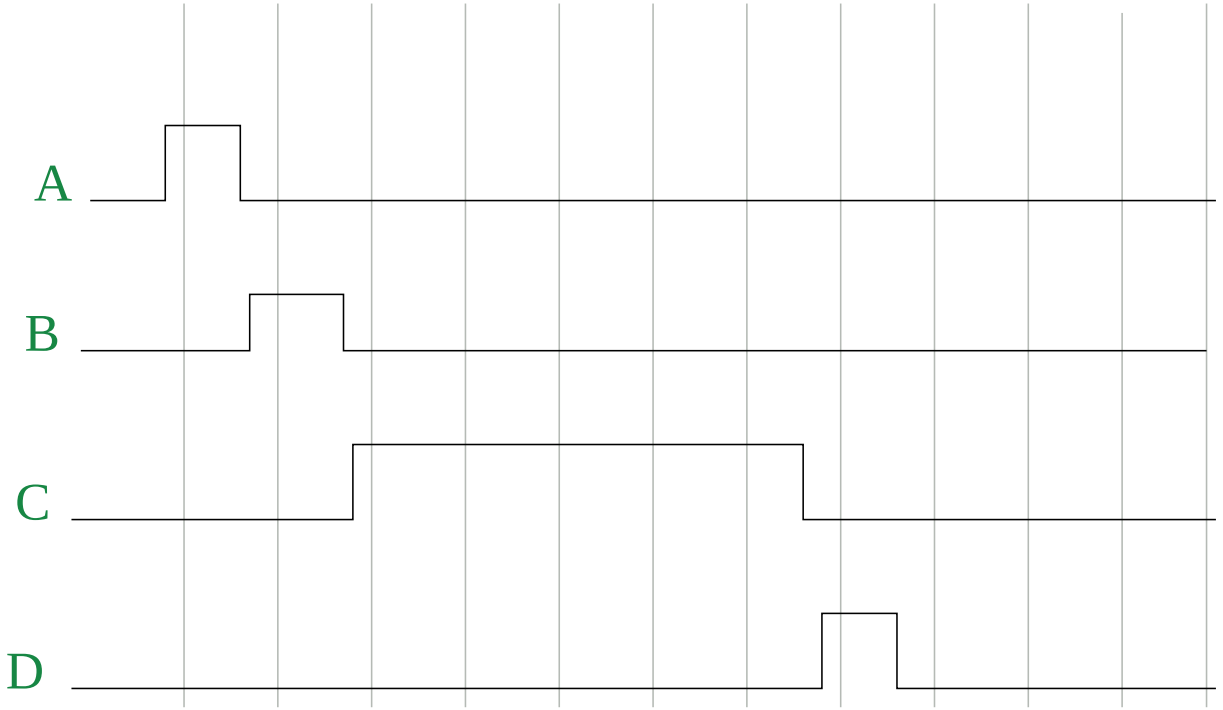
Outlines

1. PSL
2. Monitors and Generators Construction
3. Experimental Results
4. The Horus Platform

Introductory example

Example

PSL property : **always A -> next { B ; C [*]; D}**



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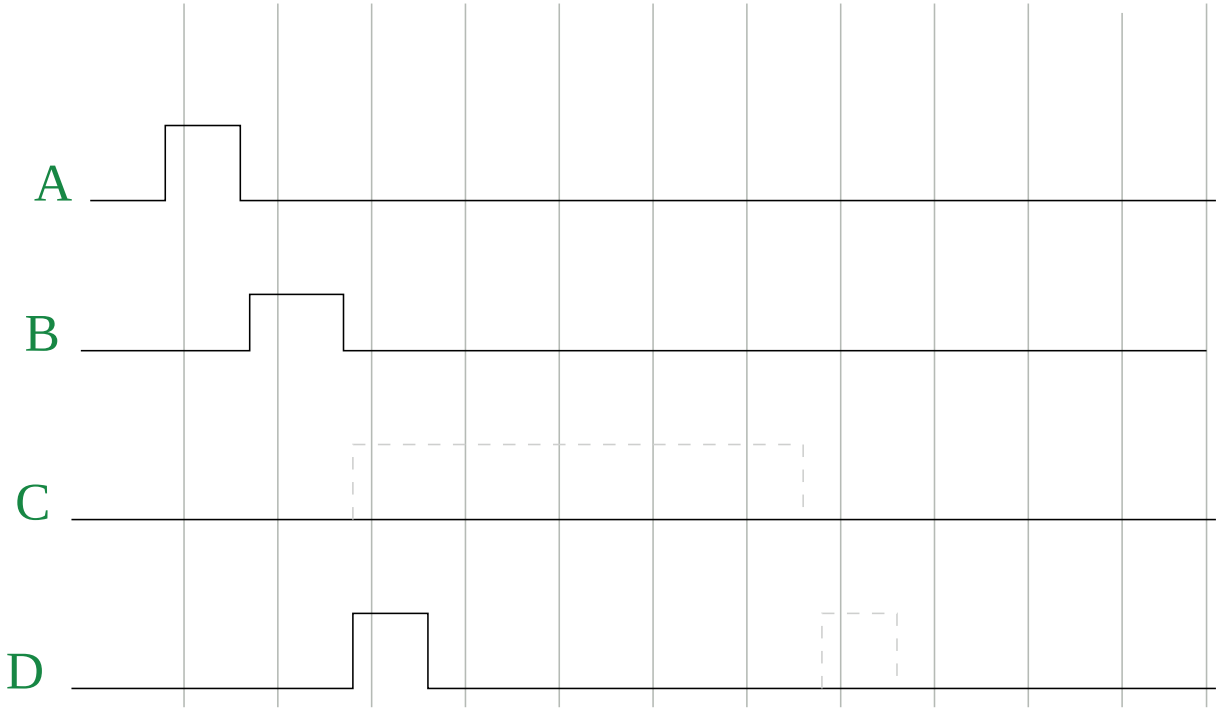

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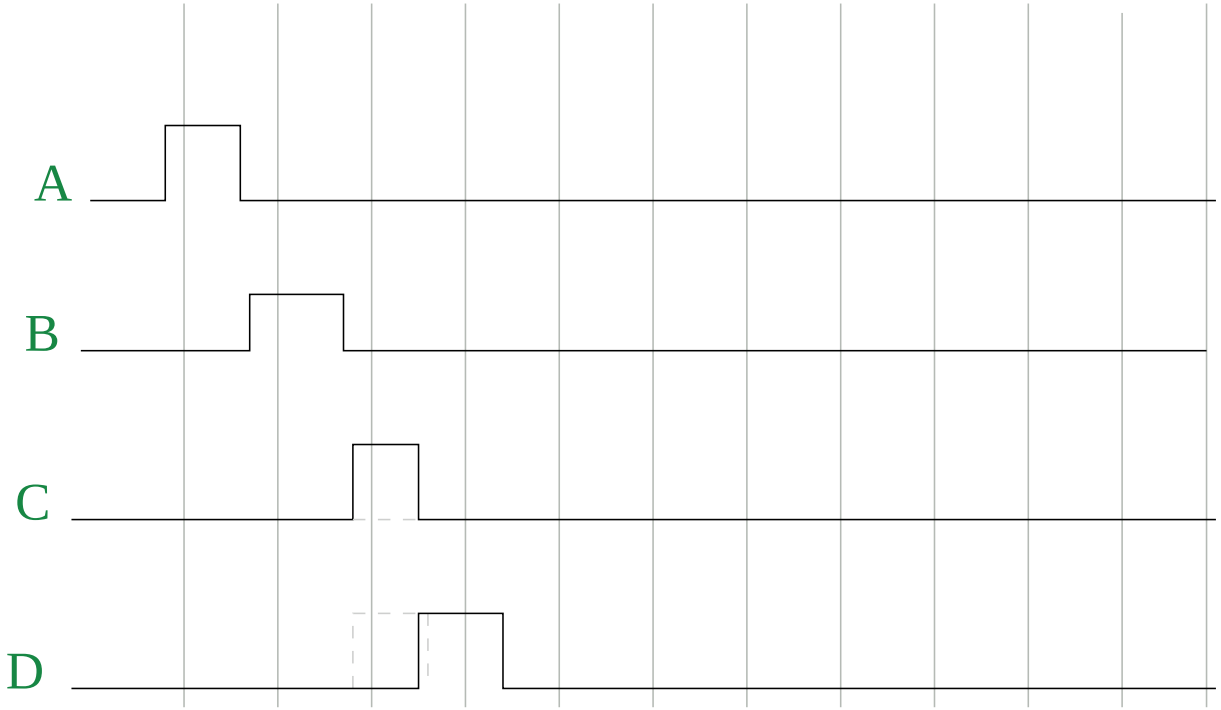

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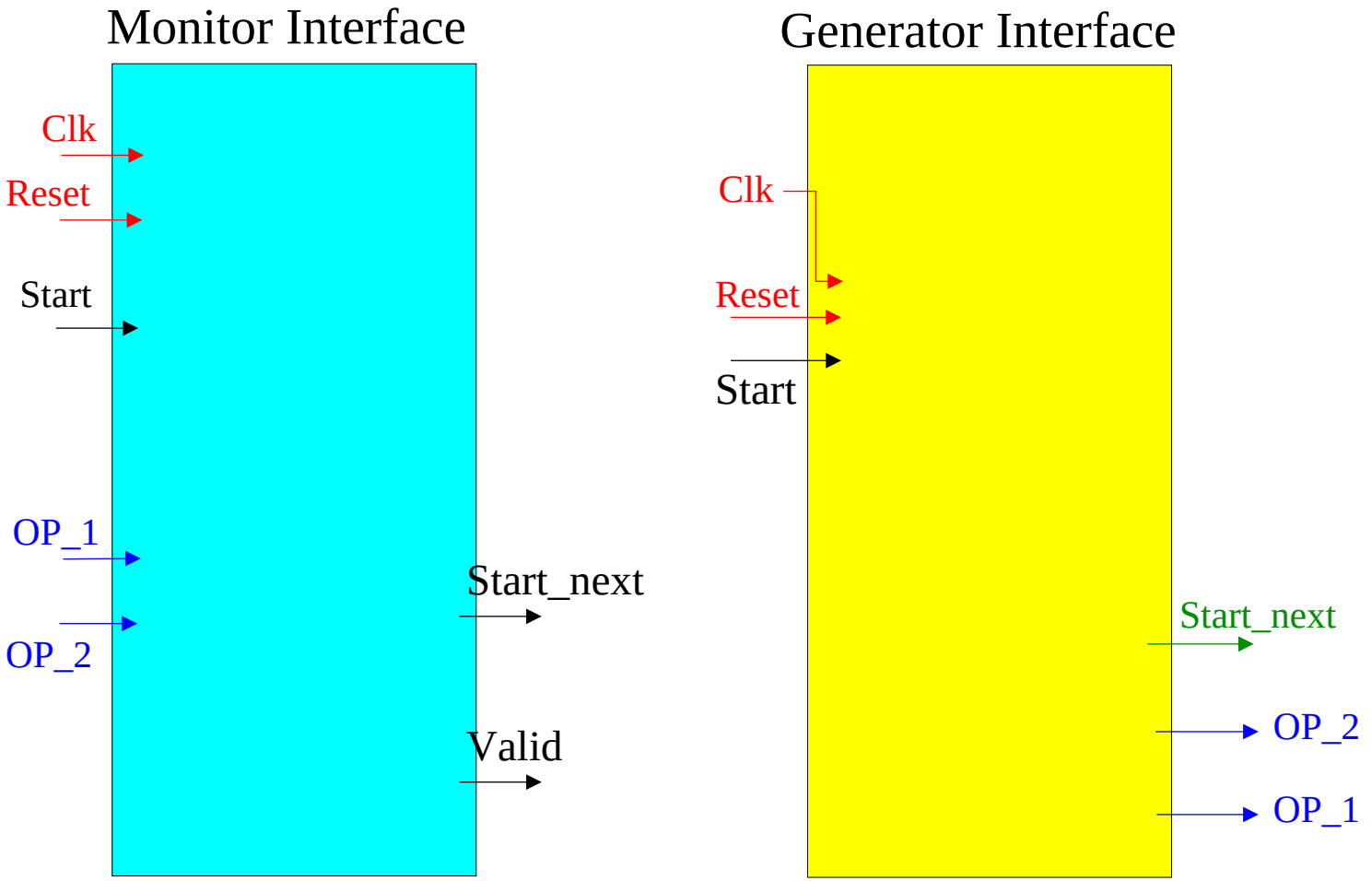
The method

Based on

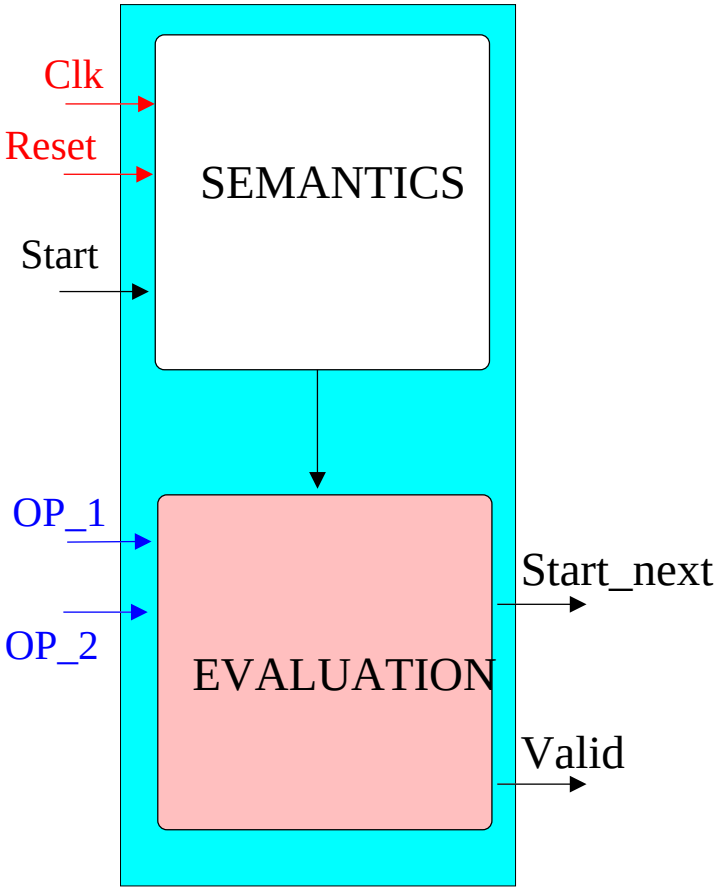
- Elementary components library
- Interconnection scheme: Syntax directed

Primitive Component

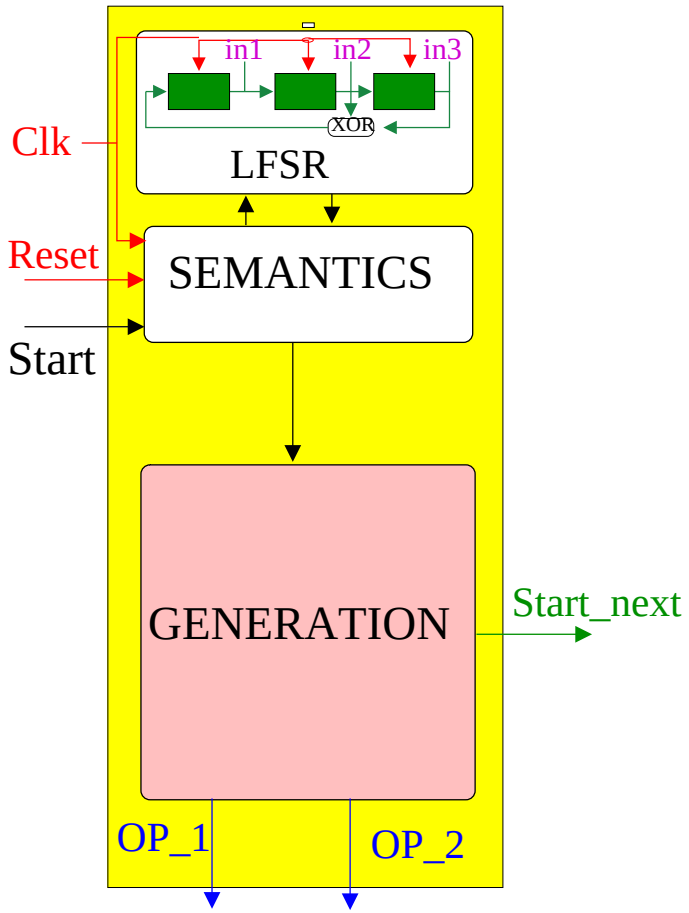


Primitive Component

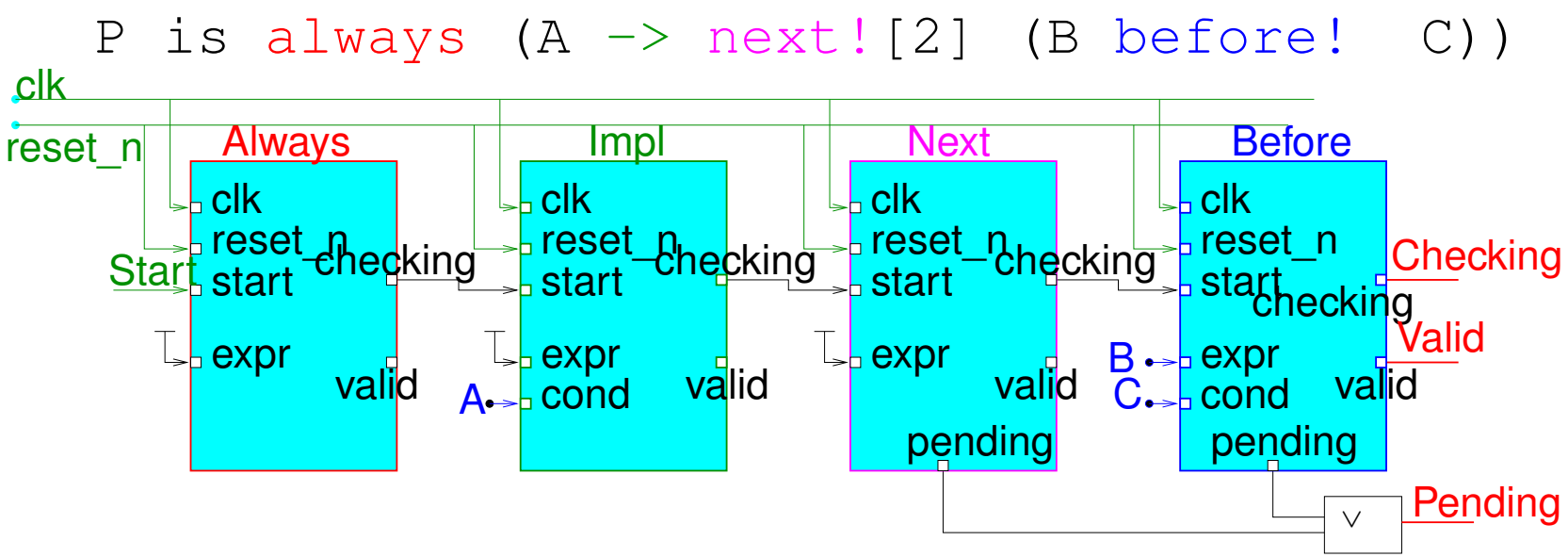
Monitor Architecture



Generator Architecture

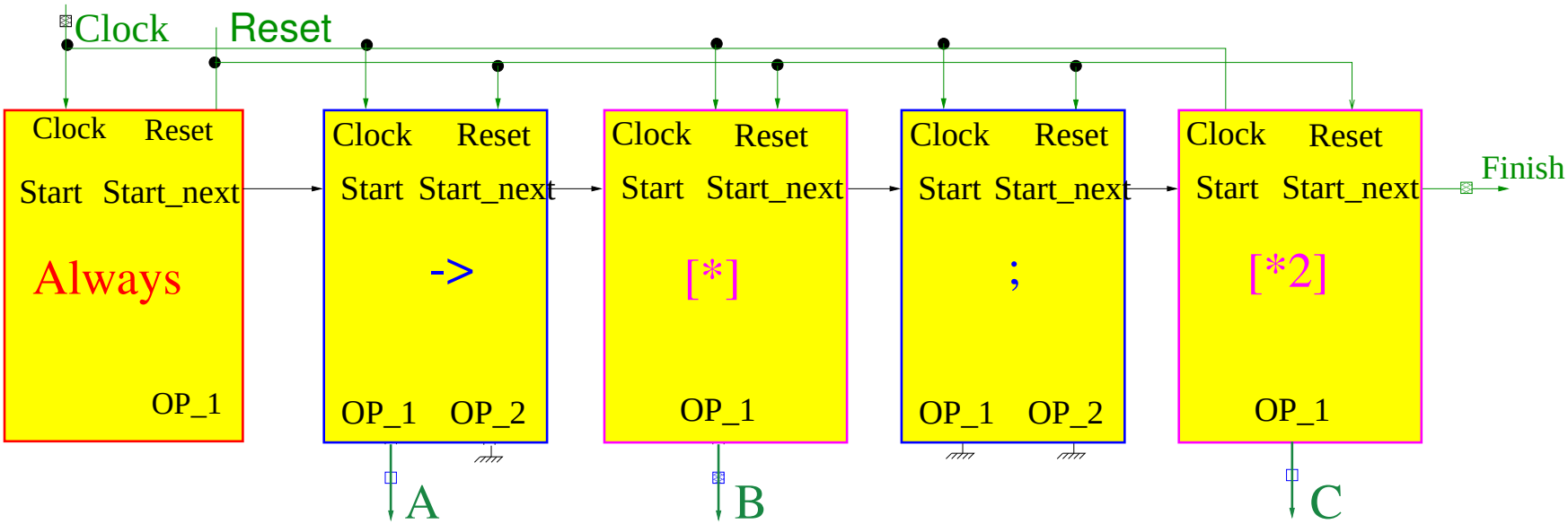


A complex monitor



A Complex Generator

always A -> { B[*] ; C[*2]}



An example: {A[+]}

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If Reset='1' then
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else if Start='1' then
    REG(timer):='1'
end if
if REG=ONE or
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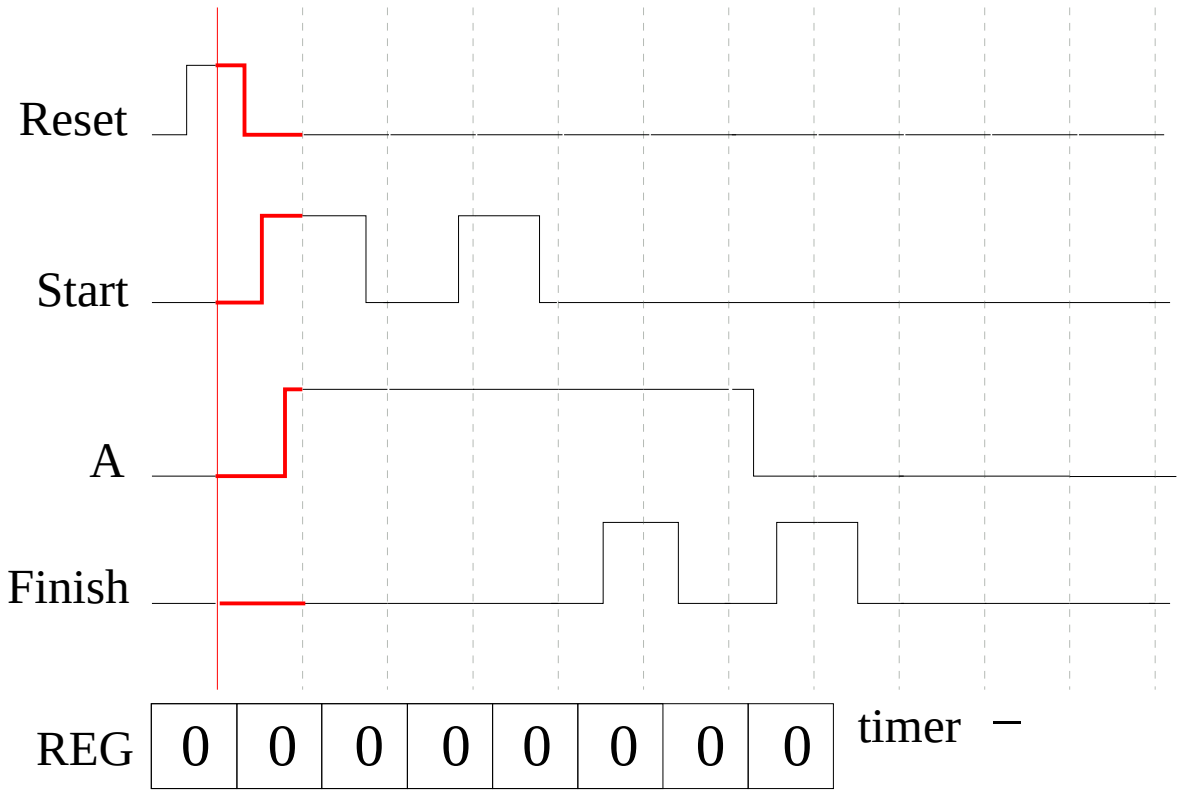
A<=Start or As;



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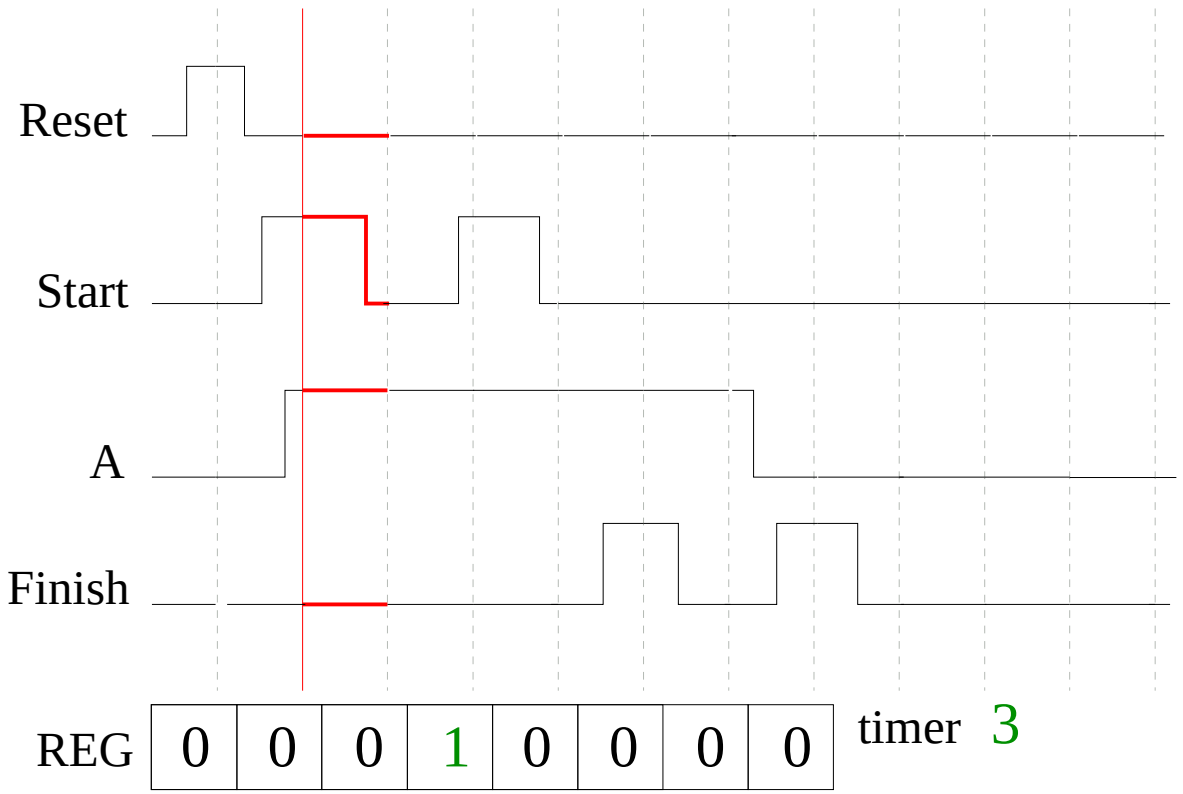

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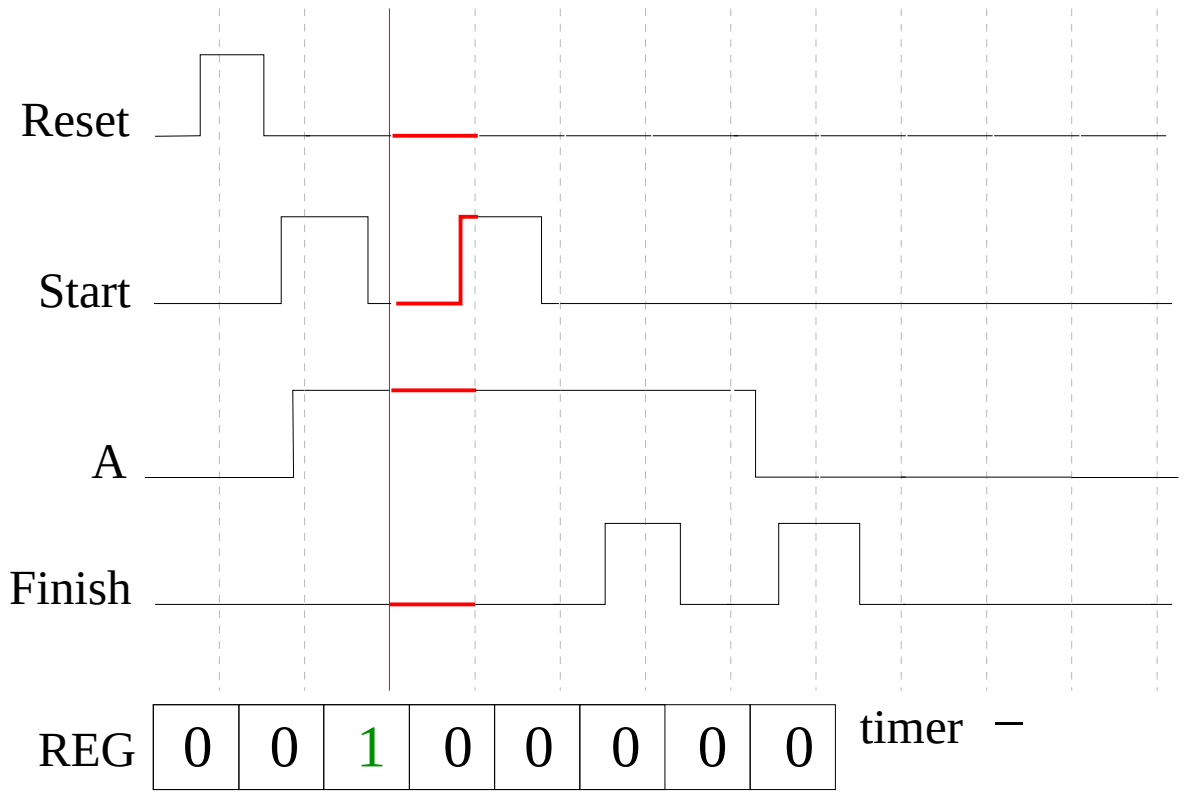

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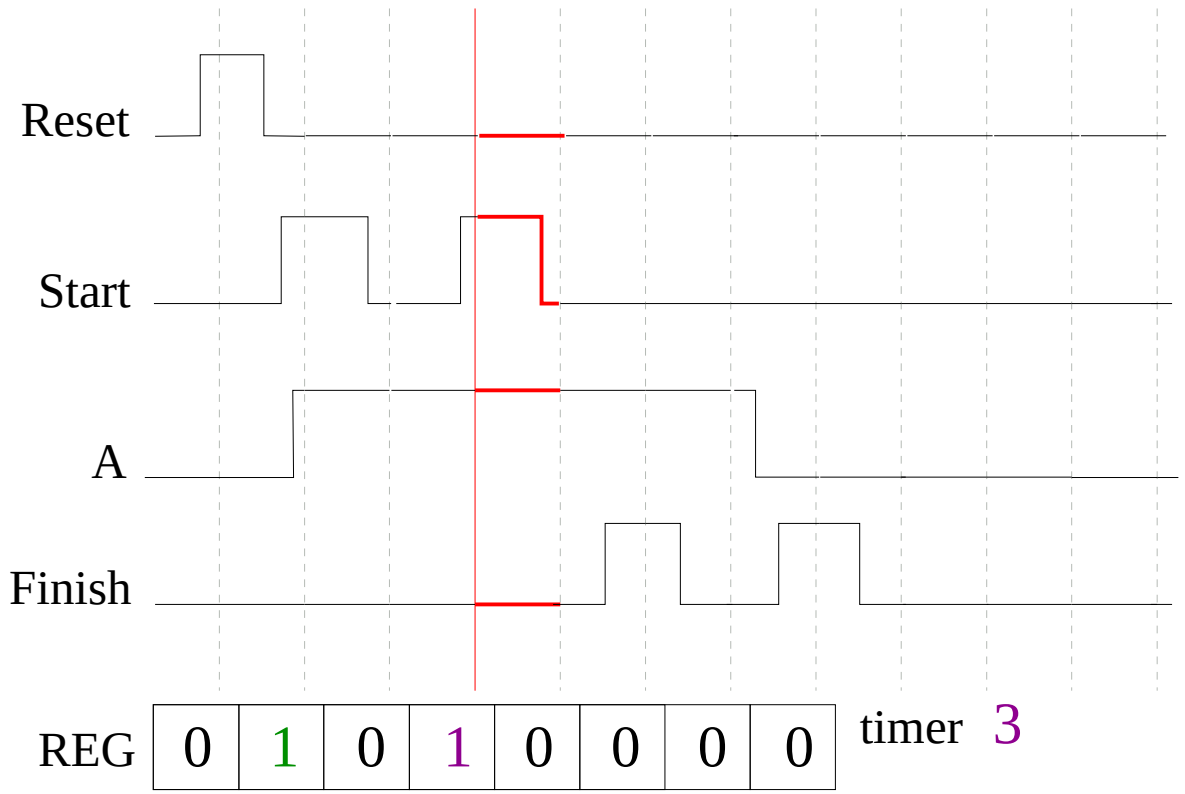

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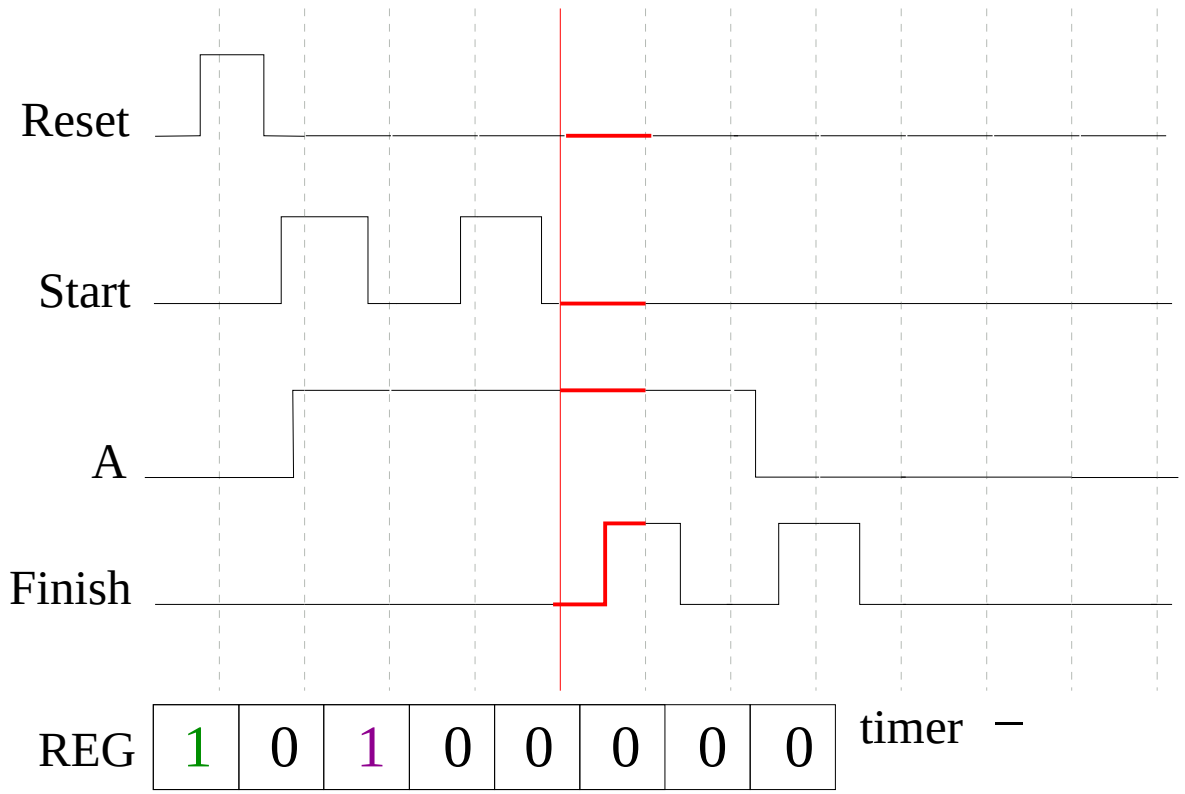

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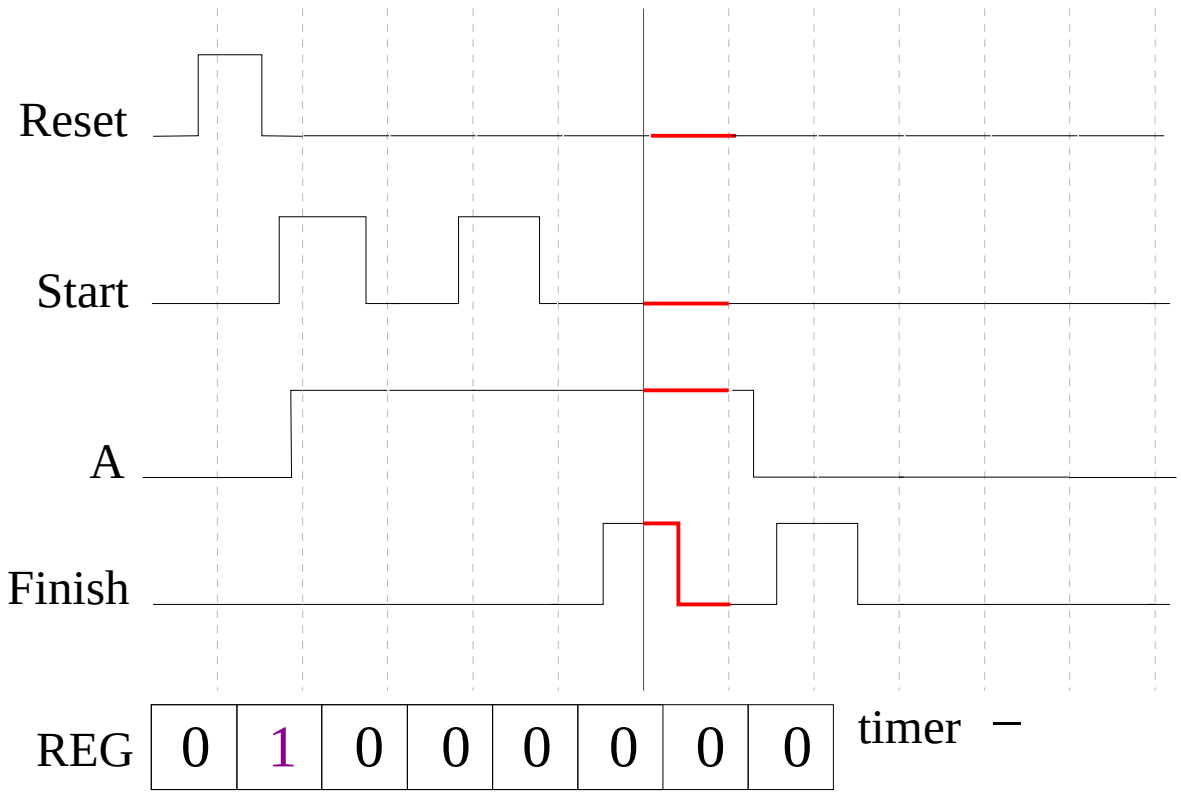

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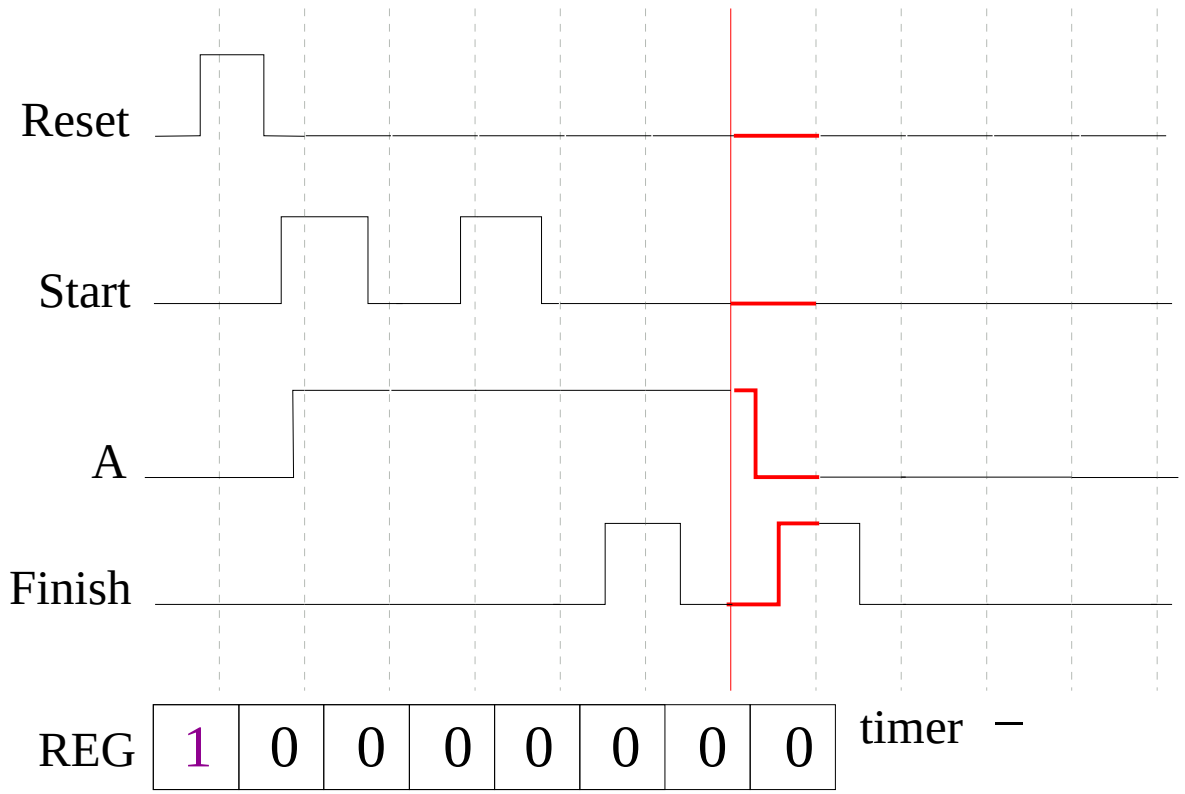

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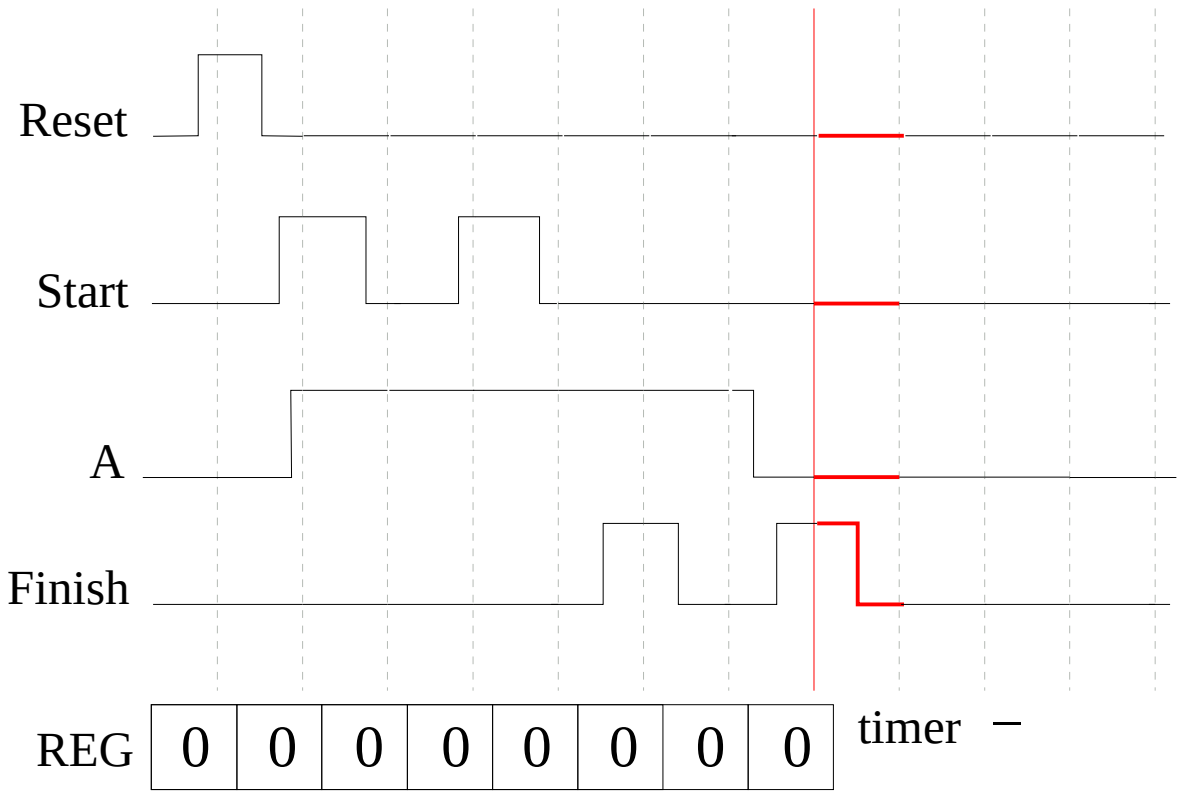

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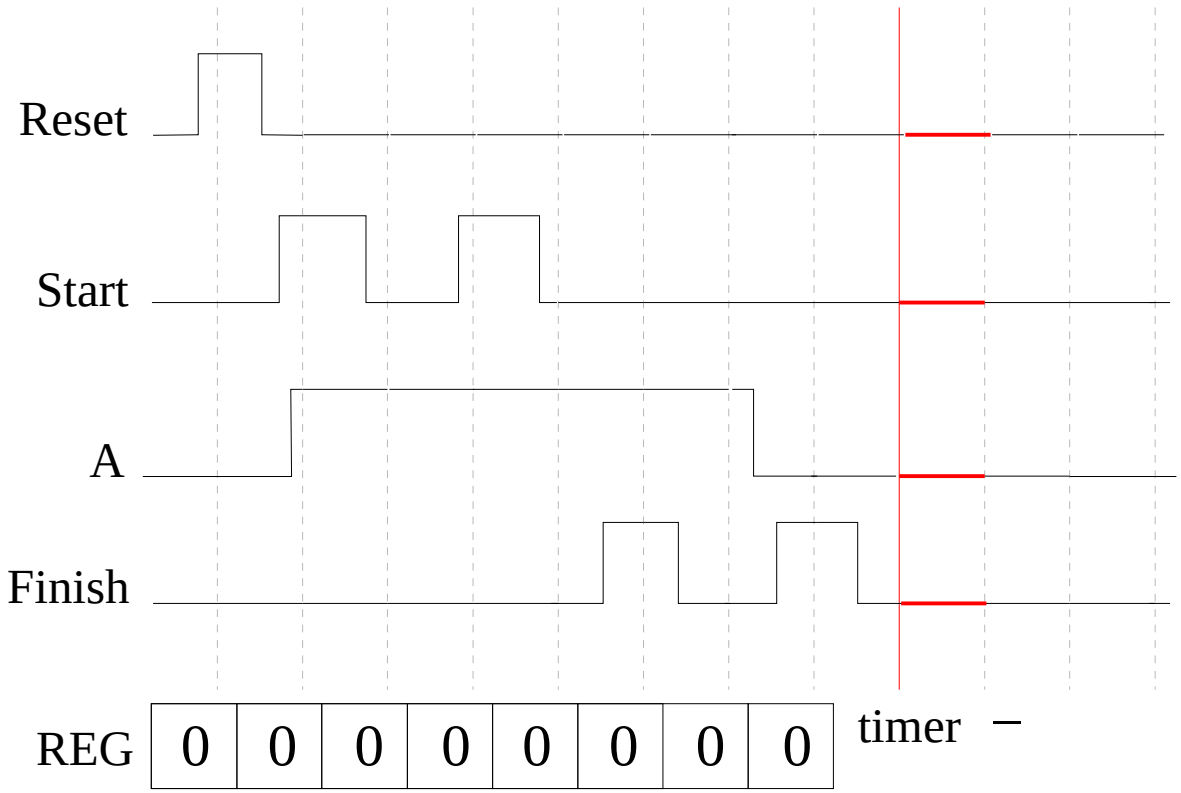

Validation

Monitors:

- FL: formal verification of the library and the interconnection scheme with a theorem prover (PVS)
- SERE : definition of a formal model based on Petri net, formal verification in progress.

Generator

- Simulation of a monitor and a generator
- Model Checking of the library
- To do: formal verification

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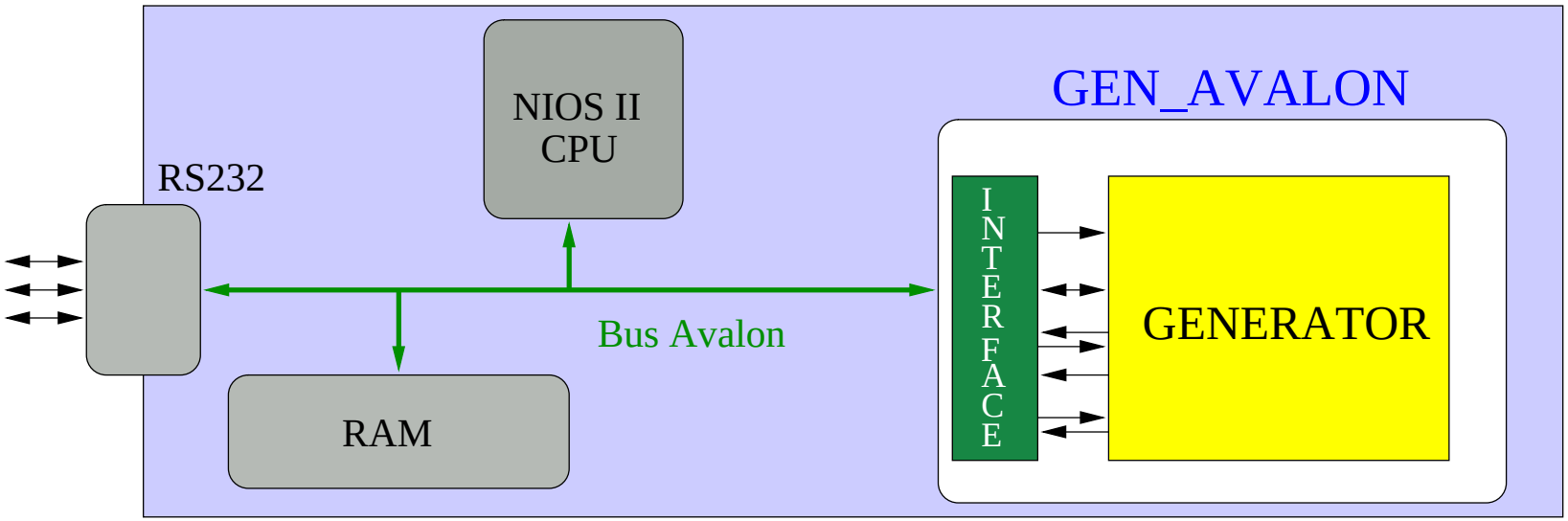
Emulation: NIOS Architecture

Complexity: CPU+RS232+RAM

- Logic Cells: 2126
- Registers: 1036
- Frequency: 50 Mhz



Synthesis Results

Monitor

```
always a -> ({b;c} until!  d)
```

- Reg: 5, LC: 8, Freq.: 439 MHz

Generator

```
always a -> next_a[4 to 8](a and b)
```

- Reg: 29, LC: 41, Freq.: 78 Mhz

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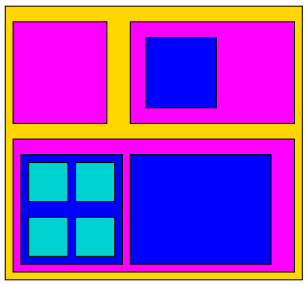
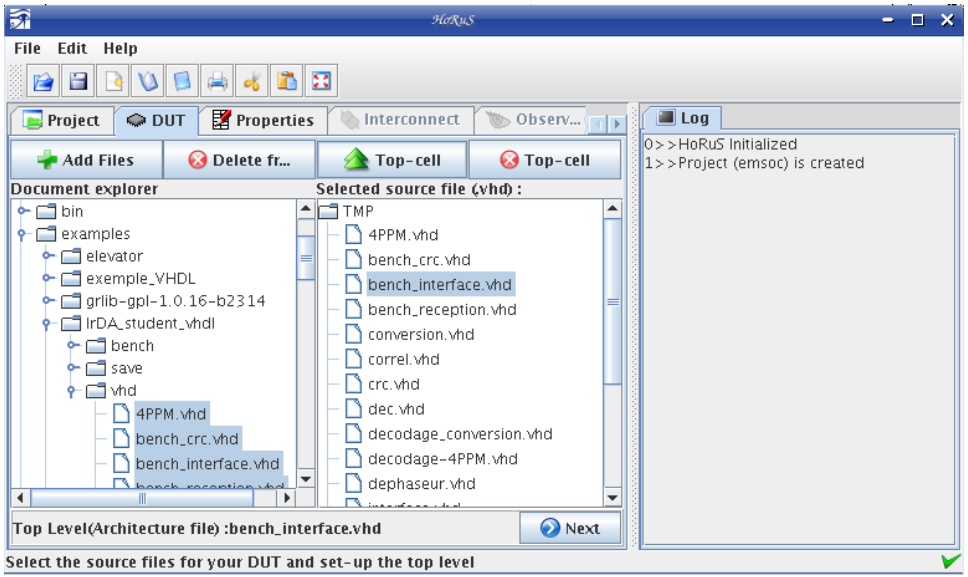
Principle

Step 1 : Load the files of the DUT

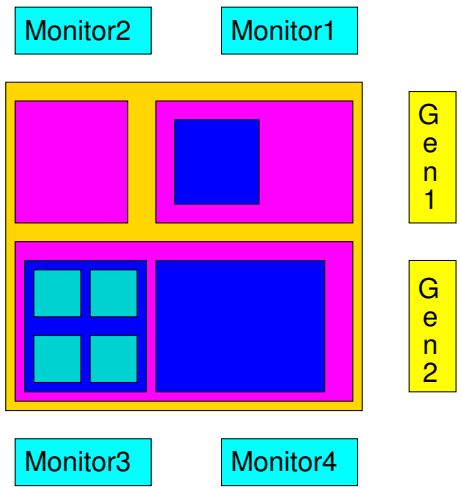
TOP Level

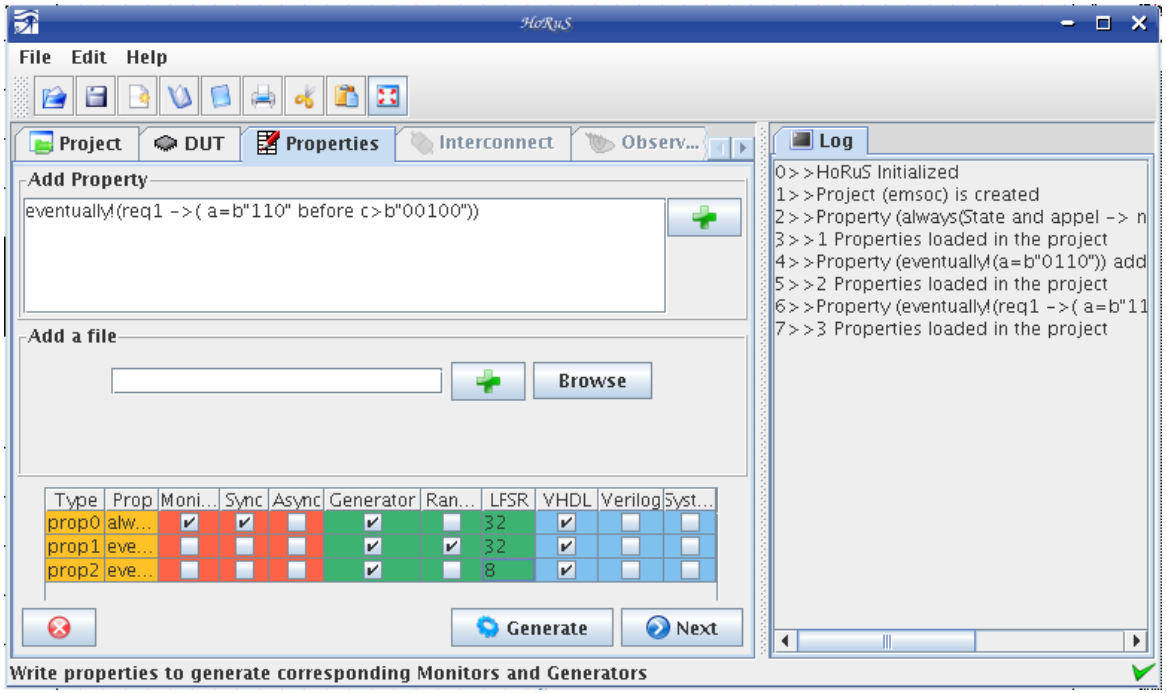




Principle

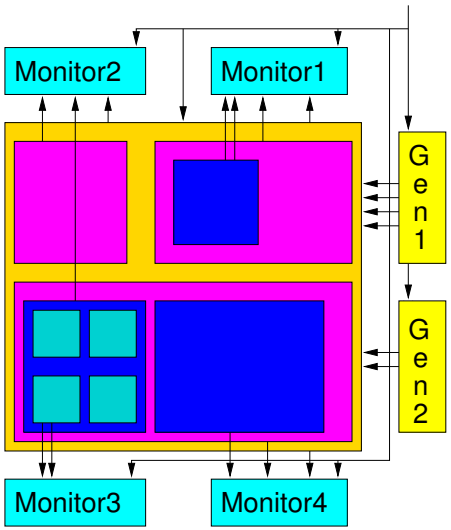
Step 2 : Produce monitors and generators from properties

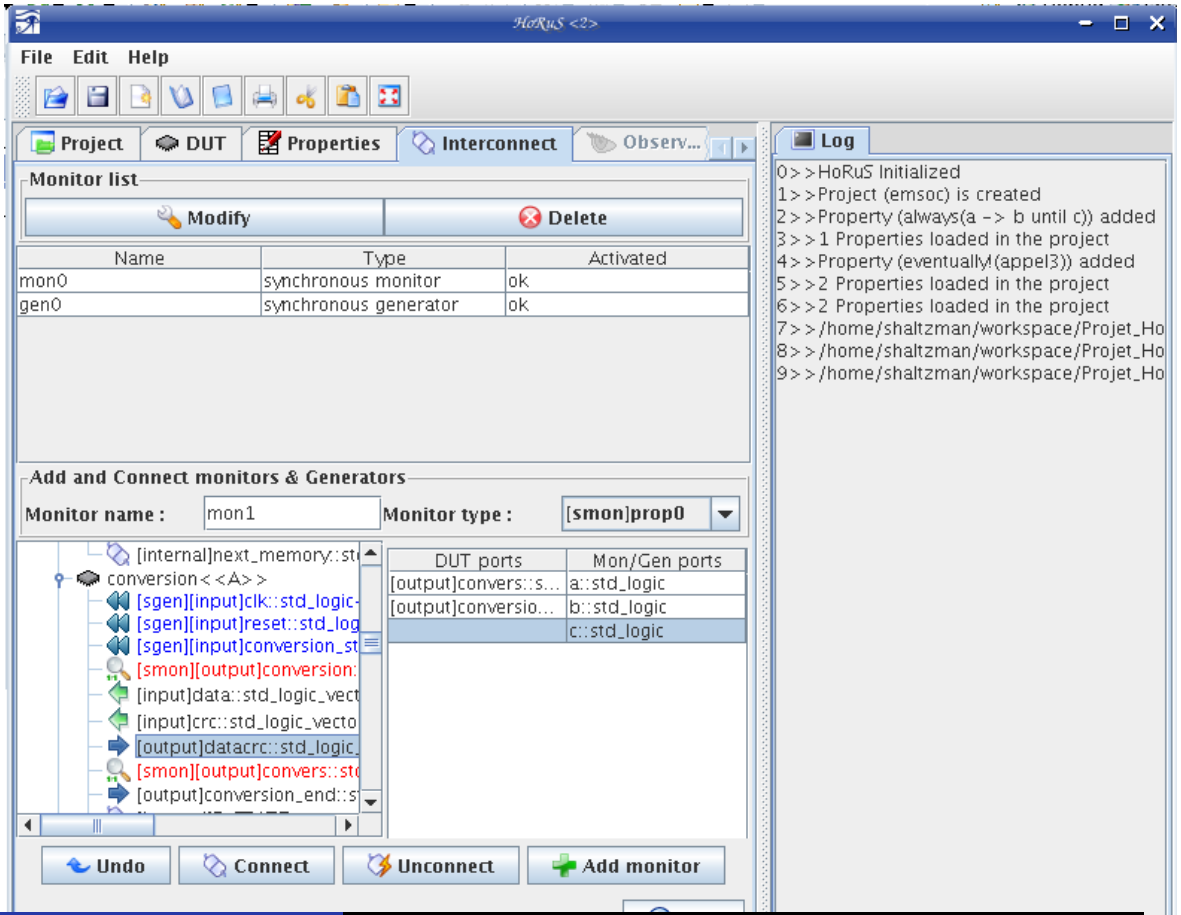




Principle

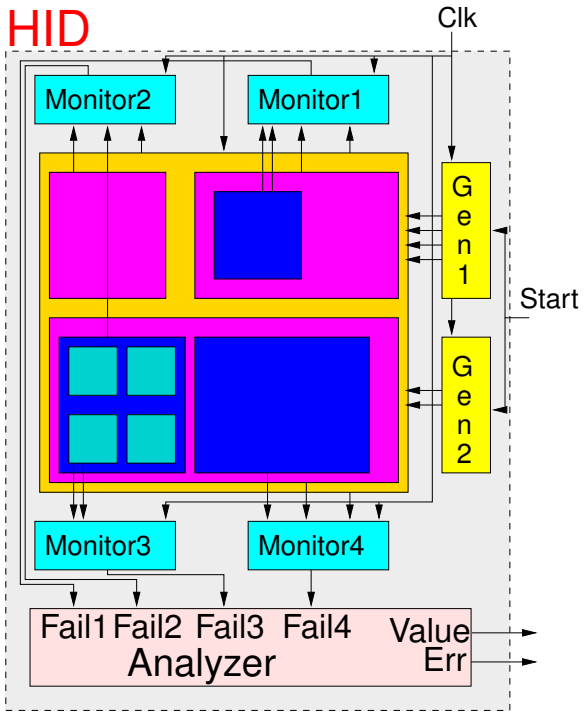
Step 3 : Connect monitors and generators to the DUT

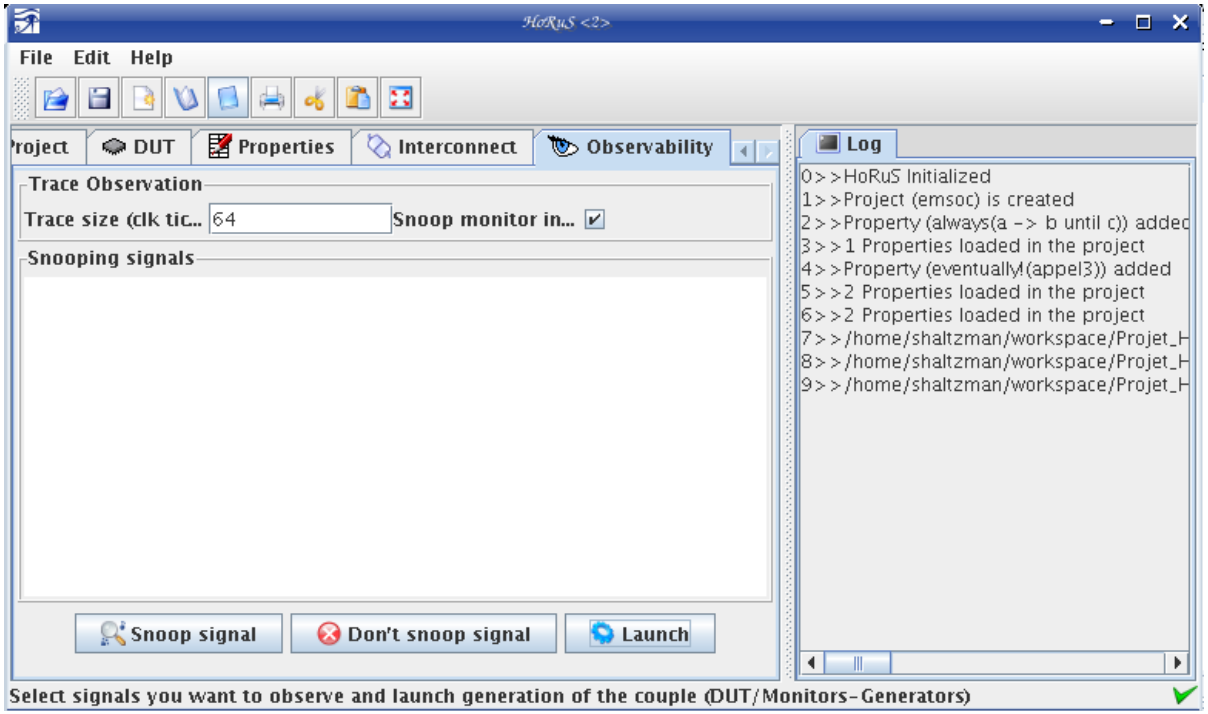




Principle

Step 4 : Build the **H**ardware **I**nstrumented **D**esign





Conclusion

- A method to generate hadware monitoror generator for PSL operators
- A platform to automatically interconnect and instrument designs
- Comparison with other tools (Focs, Dialite) for area. Our monitors are smaller

Futur Works

- Proof of correctness of generators
- Combining monitors and generators to synthesize designs
- Debug
- Extension to TLM
- Asynchronous monitoring